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YTM32B1LE0x Hardware Revision and Validation Report

YUNTU AUTOMOTIVE SEMICONDUCTOR

真车规 高可靠 高性能

Summary

Change Descripetion	Validation Plan and Conclusion
Change 1: Improvement of GPIO Noise Immunity Change 2: POR/BOR Circuit Modification Change 3: Opening of Flash Readonly Bit	1. Conducted functional and performance validation of board-level revisions on the Evaluation Board (EVB), and the results meet the design revision expectations 2. Conducted supplementary reliability validation with reference to ZVEI standards, and the results comply with AEC-Q100 requirements and design specifications 3. Conducted small-batch trial production validation of the revised materials; the CP yield of the revised batch is consistent with that of the mass-produced batch before revision, with no abnormalities **4. No abnormal feedback from other customer verifications**

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01 Hardware Revision Description

Change 1: Improvement of GPIO Noise Immunity

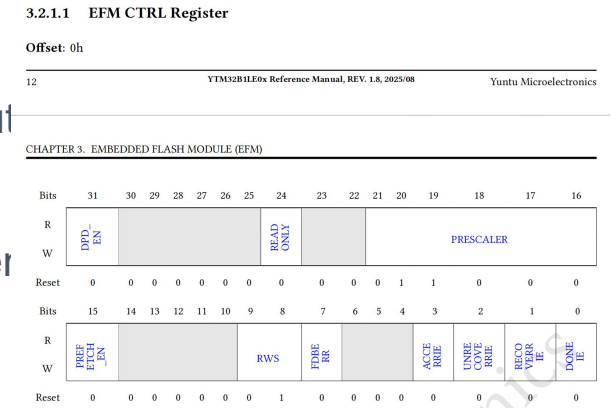
- **Revision and Purpose:**
  - Modification: Increased the input noise immunity of GPIO smit from 50mV to 500mV.
  - Purpose: Enhance the noise immunity of GPIO smit during VIL/VIH input levels and fix Errata Sheet E300001.
- **Hardware Compatibility:**
  - The GPIO modification only improves the noise immunity of GPIO to external input signals, without affecting other functions of GPIO, such as input/output characteristics, pull-up/pull-down, leakage current, etc. No targeted modifications are required for peripheral hardware.
- **Software Compatibility:**
  - For the fix in Errata Sheet E300004 that requires enabling the digital Filter function for the edge change of GPIO input signals, it remains effective after the revision, and no modifications are needed.
  - For systems without the scenario described in E300004, no software modifications are required.

Change 2: POR/BOR Circuit Modification

- **Revision and Purpose:**
  - Modification:
    - Adjusted the POR (Power-On Reset) voltage threshold
    - Forced the BOR (Brown-Out Reset) enable control signal to be valid (always enabled)
  - Purpose:
    - Solve the abnormal power-on problem caused by residual voltage in some special application scenarios
    - Improve the startup reliability and anti-interference capability of the system under power supply fluctuations and unstable power supply conditions:
- **Hardware Compatibility:**
    - The adjustment of the POR voltage threshold only affects the initialization logic of the internal reset circuit of the MCU, without impacting external hardware interfaces and the BOR voltage threshold.
    - The modification will not affect the original power supply design, and the original hardware scheme can be retained.
    - For application scenarios where a pull-down resistor was added to the power-on circuit to avoid residual voltage before the revision, the additional pull-down measure can still be retained in the revised chip.
    - No targeted modifications are required for hardware.
- **Software Compatibility:**
    - In the revised chip, the BOR ENABLE control signal is forced to be valid and is no longer controlled by the configuration bit of the PCU module.
    - For read/write operations involving this bit in the original software, the register access behavior remains consistent, but it no longer has an actual control effect on the hardware.
    - No functional software modifications are required, and the overall compatibility is good.

Change 3: Opening of Flash Readonly Bit

- **Revision and Purpose:**
  - Modification: Document revision; the reserved bit EFM->CTRL[READONLY] in the Flash control register is now officially opened for users to configure and use.
  - Purpose: Provide users with an additional Flash erasure/writing protection function without


3.2.1.1 EFM CTRL Register

Offset: 0h

12 YTM32B1LE0x Reference Manual, REV. 1.8, 2025/08 Yuntu Microelectronics

CHAPTER 3. EMBEDDED FLASH MODULE (EFM)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	DPD_EN							READONLY			PRESCALER					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PREFETCH_EN						RWS		FDBEIR				ACCEIRE	UNREECCIRE	RECOVERRIE	DONEIE
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

- **Hardware Compatibility:**
  - This modification is a document revision and does not involve MCU changes; no customer required.
- **Software Compatibility:**
  - To use this function, the software needs to write 1 to the READONLY bit of the EFM module's CTRL register. Before performing normal Flash erasure/writing, write 0 to this bit first, and write 1 to it after completion to achieve complete protection.
  - Note: The EFM->CTRL[READONLY] register only supports write operations; any read operation will return 0.
  - Note: After enabling the Flash READONLY protection, the original Flash erasure and writing functions will not return errors, and the software needs to add result verification.
  - The corresponding software modifications have been updated in the latest SDK version YTM32B1LE0 1_3_1_HF001, which can be downloaded through the YCT tool.
  - For previous versions, refer to https://forum.ytmicro.com/topic/1054/efm-readonly-bit使用说明 (EFM READONLY Bit Usage Instructions) for modifications.

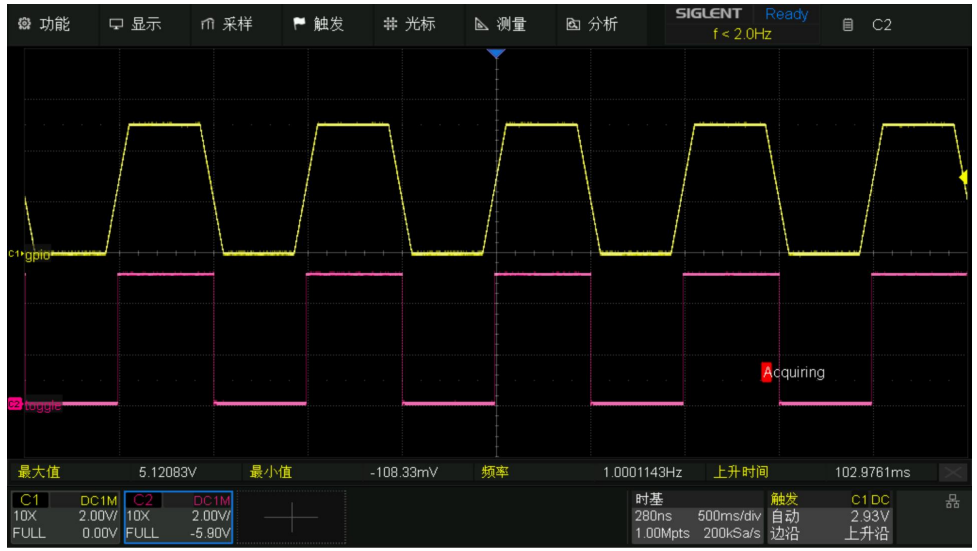
02 Hardware Revision Validation Report

02-1 Hardware Revision Validation Report_EVB

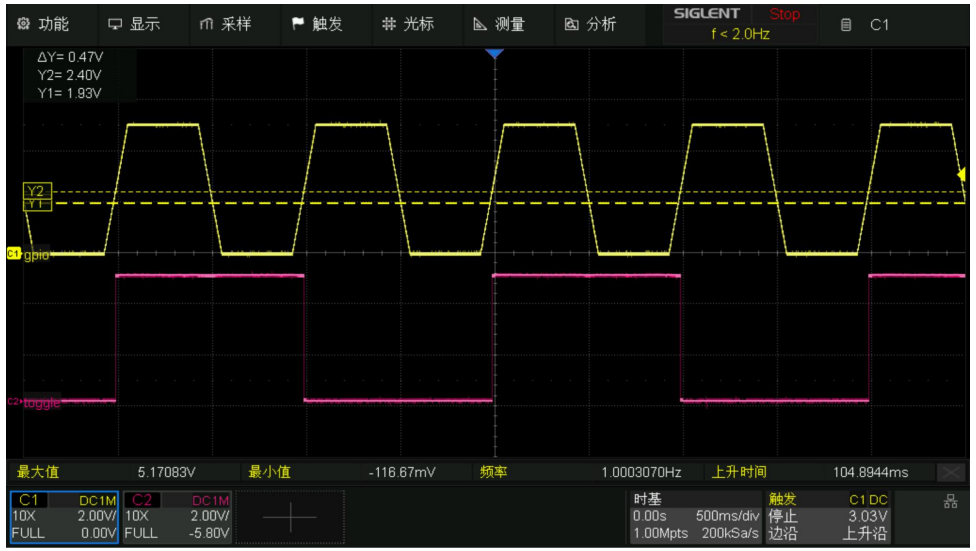
Validation Report 1: Improvement of GPIO Noise Immunity

Validation Plan:

- Conducted a single IO test to check the abnormal triggering of GPIO edges under edge change conditions of 1ns, 1us, 10us, 100us, 1ms, 10ms, 100ms, and 1s, and compared with the chip before revision.
  - The test shall ensure that no abnormal interrupt triggering occurs on the IO under the above waveforms.
  - The test shall determine an abnormal triggering edge by comparing with the chip before revision (typical value: 1ms), and test the operation of other IOs under this edge.
- The modification involves all GPIOs; therefore, all other IOs need to be tested with the above edges, and all IOs shall work as expected.



Before revision: The IO was configured to trigger an interrupt on the rising edge; an abnormal falling edge trigger occurred due to an excessively slow IO edge, which did not meet the design expectations.



After revision: The IO was configured to trigger an interrupt on the rising edge; only the rising edge triggers the interrupt even if the IO edge is excessively slow, which meets the design expectations.

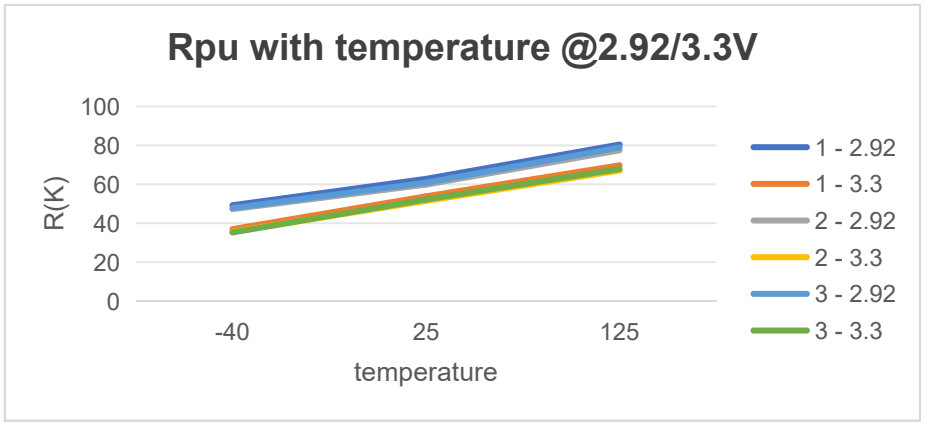
验证结论Validation Conclusion:

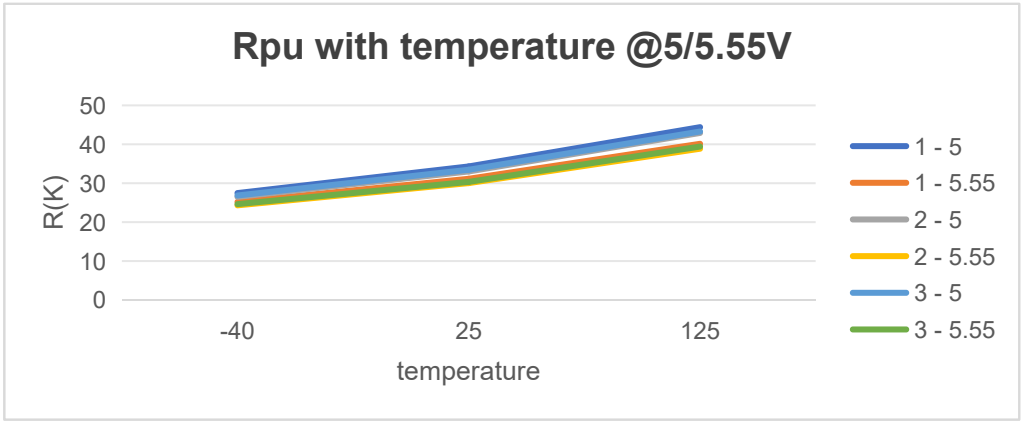
- After the modification, no abnormal interrupt triggering occurs on the IO when the IO edge ranges from 1ns to 1s.
- All IOs have been verified to have no abnormal interrupt triggering.
- The modification meets the design revision expectations, and the test results are normal.

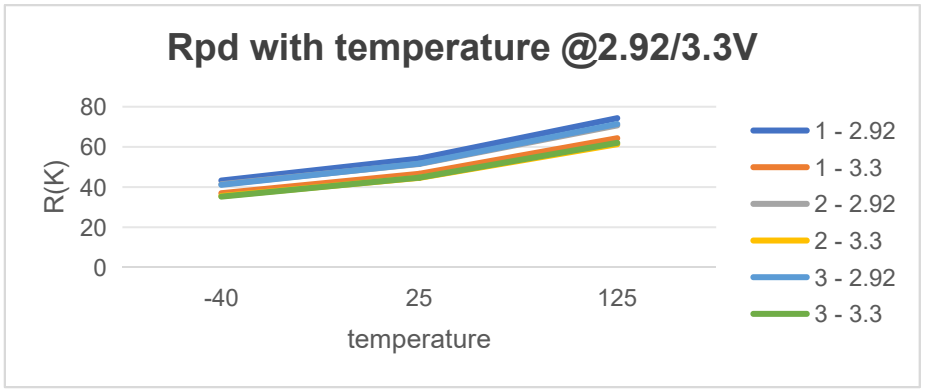
Validation Report 1: GPIO Pull-Up/Pull-Down Resistor Test

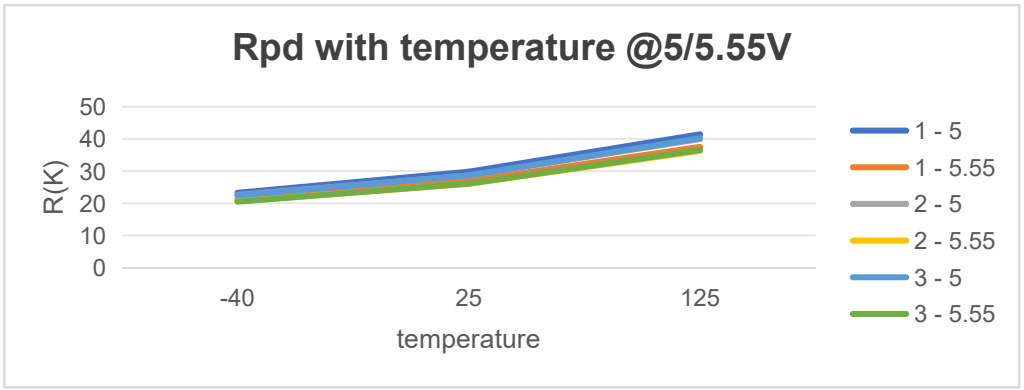
Validation Plan:

- To test the GPIO pull-up resistor: Configure the GPIO to enable pull-up, short-circuit the external ammeter to ground to record the current, and calculate the pull-up resistor based on the VDD voltage and current value.
- To test the GPIO pull-down resistor: Configure the GPIO to enable pull-down, short-circuit the external ammeter to VDD to record the current, and calculate the pull-down resistor based on the VDD voltage and current value.









Validation Conclusion:

- After the revision, Rpu and Rpd comply with the Datasheet and are consistent with those before the revision.

R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

3.3V Datasheet Spec

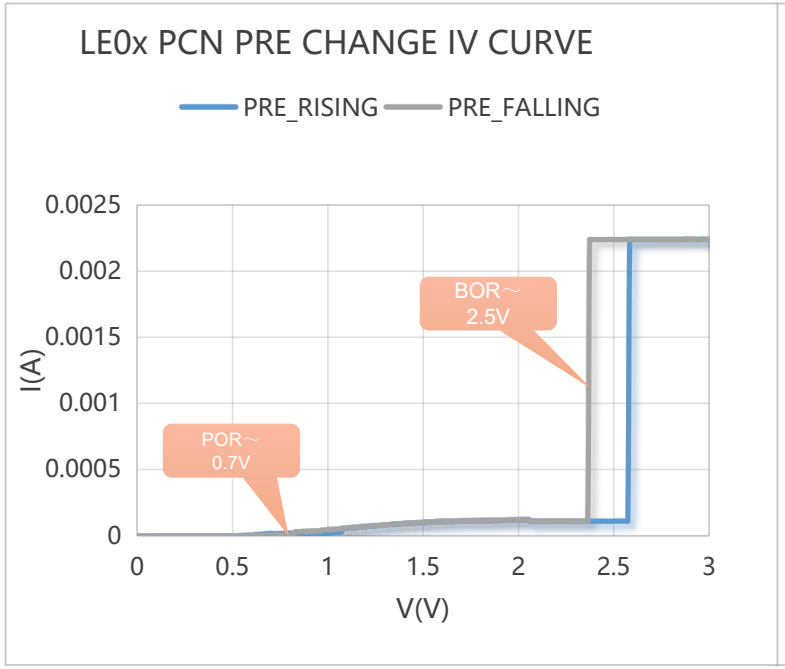
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	15	–	70	kΩ	

5V Datasheet Spec

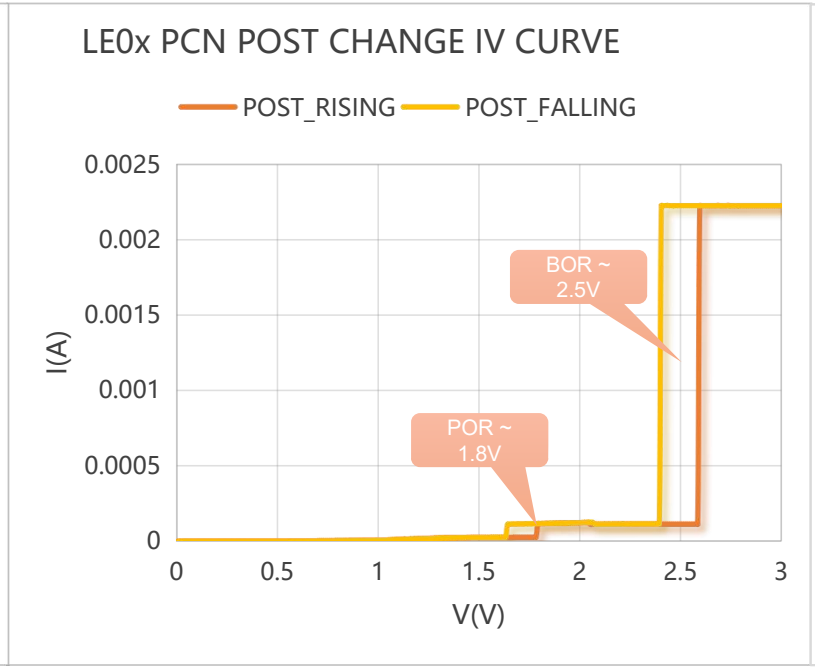
Validation Report 2: Adjustment of POR Voltage

Validation Plan:

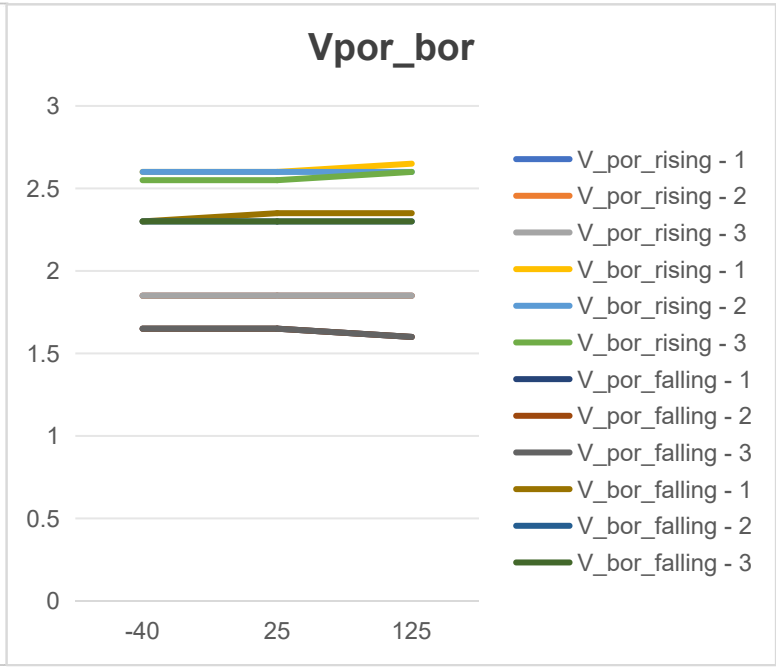
- Determined the POR and BOR trigger voltages of the chip by testing the IV curve, and verified whether the POR and BOR voltages have corresponding hysteresis.



Before revision: POR voltage < 1V, BOR voltage ≈ 2.5V



After revision: POR voltage ≈ 1.8V, BOR voltage ≈ 2.5V; both POR and BOR have obvious hysteresis.



After the revision, the POR voltage and BOR voltage are stably distributed.

Validation Conclusion:

- After the revision, the POR voltage has changed from the original threshold of less than 1V to approximately 1.8V, which meets the design revision expectations.

Validation Report 2: BOREN Control Bit Forced Valid

Validation Plan:

- Supply external VDD of 5V (V1) to the MCU.
- Modify the software to set PCU->BORCR[BOREN] = 0 (for testing only; keep PCU->BORCR=0x01U in actual applications).
- Clear the RCU->RSSR register through software.
- Reduce the MCU supply voltage to V2 and maintain it for 5ms.
- Raise the MCU VDD supply voltage back to 5V (V1).
- Read the RCU->RSSR register through software to check if the POR_BOR bit is set.
- Adjust the V2 voltage in the range of 3V to 0V, and record the V2 value when the POR_BOR bit is set.

Validation Result:

- Before revision: Under the condition of BOR detection disabled, the POR_BOR trigger voltage is approximately 0.8V, which is consistent with the POR trigger voltage.
- After revision: Under the condition of BOR detection disabled, the POR_BOR trigger voltage is approximately 2.5V, which is consistent with the BOR trigger voltage.
- After revision: Under the condition of BOR detection disabled, the test chip can stably trigger BOR reset at 2V, indicating that BOR cannot be disabled by software.

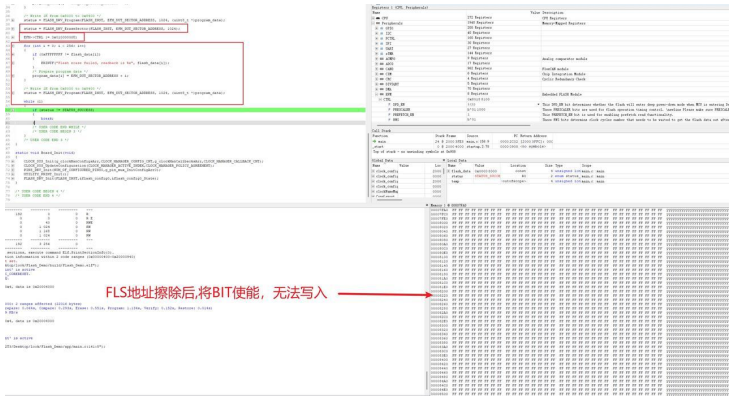
Validation Conclusion:

- After the revision, writing to the PCU->BORCR[BOREN] register through software cannot disable the BOR detection circuit, which is consistent with the design revision expectations.

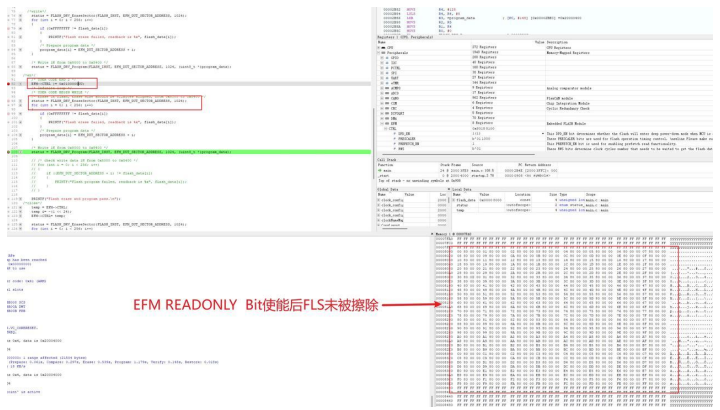
Validation Report 3: Document Revision, Opening of Flash READONLY Function

Validation Plan:

- he software sets EFM->CTRL[READONLY] to 0 (disabled) and performs Flash erasure/writing operations; the corresponding address of Flash in the Memory Map should be erasable and writable normally.
- Keep the corresponding address of Flash in the erased state, set EFM->CTRL[READONLY] to 1 (enabled) through software, and perform Flash writing operations; the corresponding address of Flash in the Memory Map should remain in the erased state.
- Keep the corresponding address of Flash in the programmed state, set EFM->CTRL[READONLY] to 1 (enabled) through software, and perform Flash erasure operations; the corresponding address of Flash in the Memory Map should remain in the programmed state, and the original data should not be erased.



READONLY enabled: Flash cannot be Programmed



READONLY enabled: Flash cannot be Erased

READ ONLY	Program	Erase
0	Y	Y
Write 1 (Read0)	N	N

READONLY Truth Table

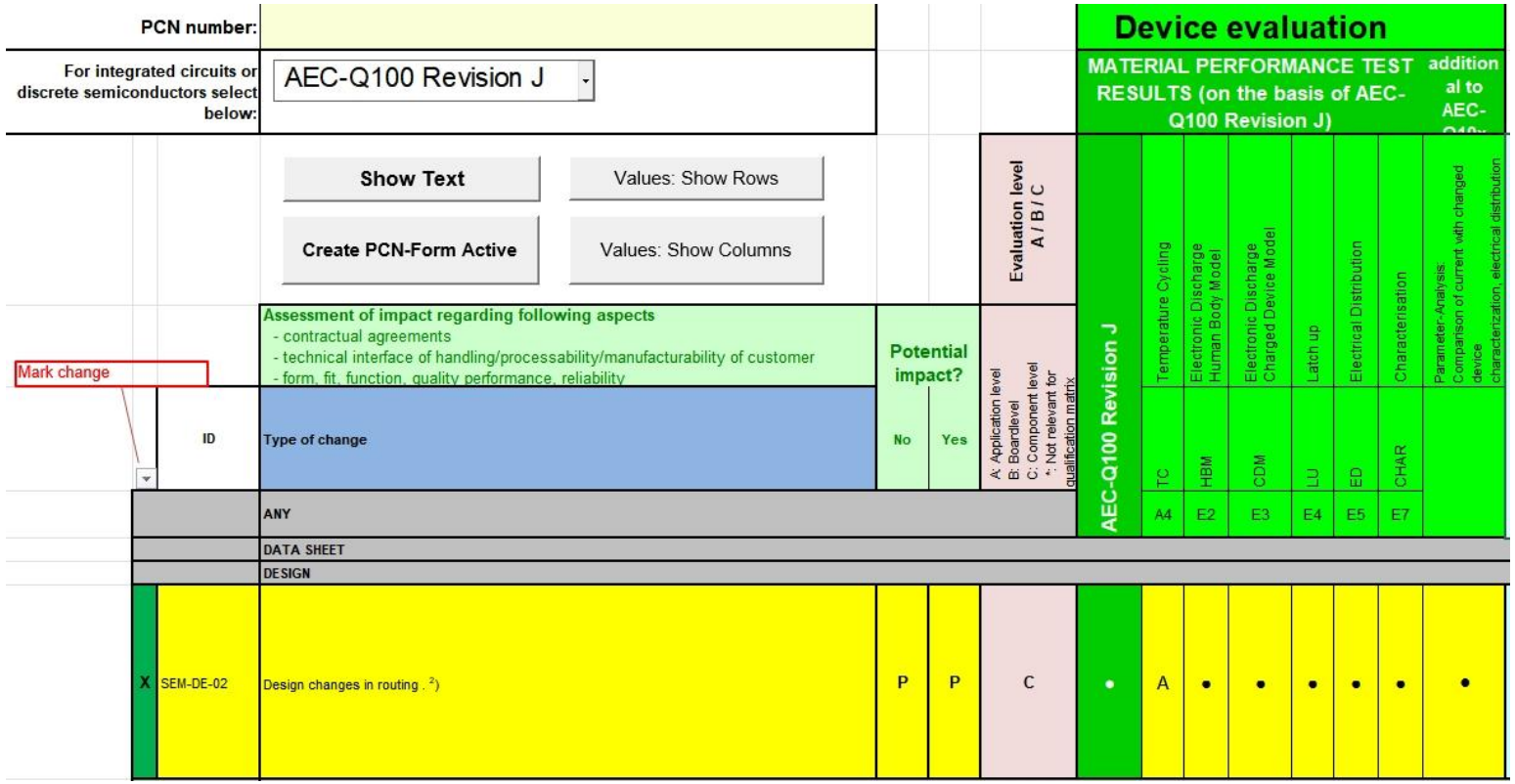
Validation Conclusion:

- When the EFM->CTRL[READONLY] bit is enabled, it can protect the Flash content from being erased and written; when the EFM->CTRL[READONLY] function is disabled, the Flash can be erased and written normally. This function can effectively protect the Flash content from abnormal modifications.

02-2 Hardware Revision Validation Report_ZVEI Supplementary Reliability Validation

ZVEI Supplementary Reliability Validation

- **Validation Plan:**
  - Evaluated by ZVEI: A4/E2/E3/E4/E5/E7 are the items requiring verification.



PCN number:					Device evaluation								
For integrated circuits or discrete semiconductors select below:	AEC-Q100 Revision J				MATERIAL PERFORMANCE TEST RESULTS (on the basis of AEC-Q100 Revision J)								addition al to AEC-Q10x
	Show Text / Values: Show Rows / Create PCN-Form Active / Values: Show Columns			Evaluation level A / B / C	AEC-Q100 Revision J	Temperature Cycling	Electronic Discharge Human Body Model	Electronic Discharge Charged Device Model	Latch up	Electrical Distribution	Characterisation	Parameter-Analysis: Comparison of current with changed device characterization, electrical distribution	
Mark change	ID	Type of change	Assessment of impact regarding following aspects - contractual agreements - technical interface of handling/processability/manufacturability of customer - form, fit, function, quality performance, reliability	Potential impact? No / Yes	A: Application level B: Boardlevel C: Component level *: Not relevant for qualification matrix		TC	HBM	CDM	LU	ED	CHAR	
		ANY					A4	E2	E3	E4	E5	E7	
		DATA SHEET											
		DESIGN											
X	SEM-DE-02	Design changes in routing , [2])		P / P	C	•	A	•	•	•	•	•	•

ZVEI Supplementary Reliability Validation--A4

Validation Plan:

- PC + TC_1000 cycles
  - Sample size: 77 units * 1 batch
  - Temperature range: -55℃ ~ 150℃, 1000 cycles
- Results: 0 failures
- Specific verification steps:
  - STEP1: Appearance + SAT
  - STEP2: PC (Baking at 125℃ for 24 hours + Moisture absorption at 30℃, 60%RH for 192 hours + IR*3 at 260℃)
  - STEP3: SAT + ATE testing (normal and high temperature)
  - STEP4: TC (-55℃ ~ 150℃) for 1000 cycles
  - STEP5: ATE testing (normal and high temperature)
  - STEP6: Output report (including experimental steps, outputs of each step, and pictures)

检验项目、检验条件和技术要求

组别或序号	检验项目		技术条件（要求）	检验样品数（只）	检验合格数（只）	检验不合格数(只)	结果	备注
E1	起点电测试		测试参数按 YTM32B1LE05H0MLFT Test SPEC 要求进行。 判据：符合详细规范规定。	80 (1#-80#)	80	0	合格	委托方测试
A1	预处理（PC）	超声检测	试验方法：JESD22-A113I-2020，J-STD-020F-2022	22 (1#-22#)	22	0	合格	-
		温度循环	试验方法：JESD22-A113I-2020 试验条件：温度-40℃-60℃、每态停留时间 15min、转换时间≤1 min、循环 5cycles 要求：试验前后应对器件外观进行检查，标识清晰，表面无机械损伤和气孔，无封装缺损、破裂、锈蚀等，引出端能识别。	80 (1#-80#)	80	0	-	-
		高温烘烤	试验方法：JESD22-A113I-2020 试验条件：温度 125℃、时间 24h 要求：试验前后应对器件外观进行检查，标识清晰，表面无机械损伤和气孔，无封装缺损、破裂、锈蚀等，引出端能识别。	80 (1#-80#)	80	0	-	-
		湿度浸润	试验方法：JESD22-A113I-2020，J-STD-020F-2022 试验条件：60%RH，30℃，192h 要求：试验前后应对器件外观进行检查，标识清晰，表面无机械损伤和气孔，无封装缺损、破裂、锈蚀等，引出端能识别。	80 (1#-80#)	80	0	-	-
		回流焊	试验方法：JESD22-A113I-2020，J-STD-020F-2022 试验条件：150～200℃@60-120S、217℃@60-150S、260℃+5/-0@30S 以上、3cycles 要求：试验前后应对器件外观进行检查，标识清晰，表面无机械损伤和气孔，无封装缺损、破裂、锈蚀等，引出端能识别。	80 (1#-80#)	80	0	-	-
		超声检测	试验方法：JESD22-A113I-2020，J-STD-020F-2022	22 (1#-22#)	22	0	合格	-
E1	中间电测试		测试参数按 YTM32B1LE05H0MLFT Test SPEC 要求进行。 判据：符合详细规范规定。	80 (1#-80#)	80	0	合格	-
A4	温度循环（TC）		试验方法：JESD22-A104F.01-2023 试验条件：温度-55℃-150℃、每态停留时间 15min、转换时间≤1 min、循环 1000cycles 要求：试验前后应对器件外观进行检查，标识清晰，表面无机械损伤和气孔，无封装缺损、破裂、锈蚀等，引出端能识别。	80 (1#-80#)	80	0	-	-
E1	终点电测试		测试参数按 YTM32B1LE05H0MLFT Test SPEC 要求进行。 判据：符合详细规范规定。	80 (1#-80#)	80	0	合格	委托方测试

Validation Conclusion:

- The TC verification result is PASS; see the attachment for the detailed report.

ZVEI Supplementary Reliability Validation-- E2/3/4

Validation Plan:

- ESD
  - HBM PASS
    - ALL TO VDD(±) -- 500V, 1000V~4000V, step:1000V
    - ALL TO VSS(±) -- 500V, 1000V~4000V, step:1000V
    - IO TO IO(±) -- 500V, 1000V~4000V, step:1000V
  - CDM PASS -- All pin ±250, ±500V; corner pin ±750V
  - LU 25℃ PASS
    - I-trigger(±) 50~200mA;step:50mA
    - Over voltage -- 5.5V~8.25V Step:0.25V
  - LU 125℃ PASS
    - I-trigger(±) 50~100mA;step:50mA
    - Over voltage -- 5.5V~8.25V Step:0.25V

Validation Conclusion:

- The ESD validation results meet the Datasheet specifications and comply with the requirements of AEC Q100.
- See the attachment for the third-party ESD report.

ZVEI Supplementary Reliability Validation-- E5

Validation Plan:

- HTOL
  - Sample size: 77 units * 1 batch
  - VDD=5.5V, Ta=125℃, 168hrs
- Results:
  - HTOL result: 0 Fail
  - ED data result: PASS
  - Compared with the average value of HTOL test parameters before revision, there is no abnormality.

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(Hestia-48LQFP) YTM32B1LE0x Electrical Distribution Report - Rev1

Parameter Name in Datasheet	Units	Temp (℃)	Lower Spec Limit (NA if no spec)	Upper Spec Limit (NA if no spec)	Time0 (Pre-HTOL) Post ECO Sample			Post-HTOL(168hrs) Post ECO Sample			Mean Drift toward LSL	Mean Drift toward USL	Time0 (Pre-HTOL) Pre ECO Sample			Post-HTOL(1000hrs) Pre ECO Sample			Mean Drift toward LSL	Mean Drift toward USL	PreECO & PostECO Mean Drift
					Avg	Std	Cpk	Avg	Std	Cpk	Drift less than +/- 15% to spec	Drift less than +/- 15% to spec	Avg	Std	Cpk	Avg	Std	Cpk	Drift less than +/- 15% to spec	Drift less than +/- 15% to spec	Drift less than +/- 15% to spec window
RPU @5V-Internal pull-up resistors	kΩ	ROOM	20.00	70.00	29.624	1.556	2.06	31.071	2.068	1.78	PASS	PASS	30.740	1.669	2.14	30.670	1.441	2.47	PASS	PASS	2.23%
RPD @5VInternal pull-down resistors	kΩ	ROOM	20.00	70.00	25.710	1.023	1.86	26.936	1.041	2.22	PASS	PASS	26.029	1.111	1.81	26.440	1.057	2.03	PASS	PASS	0.64%
RPU @3.3V-Internal pull-up resistors	kΩ	ROOM	20.00	100.00	59.304	5.020	2.61	61.287	5.869	2.20	PASS	PASS	65.420	1.569	6.50	65.867	1.541	6.52	PASS	PASS	7.64%
RPD @3.3VInternal pull-down resistors	kΩ	ROOM	20.00	105.00	49.776	5.000	1.99	52.996	6.409	1.72	PASS	PASS	55.930	1.511	7.93	56.144	1.677	7.18	PASS	PASS	7.24%
PMC Bandgap Vref=1V	V	ROOM	0.96	1.04	0.999	0.003	4.28	0.994	0.004	2.81	PASS	PASS	1.000	0.005	2.67	1.004	0.006	2.12	PASS	PASS	1.86%
FSIRC - Slow internal reference frequency	MHz	ROOM	1.94	2.06	1.998	0.005	4.17	2.000	0.006	3.11	PASS	PASS	2.000	0.010	2.00	2.004	0.010	1.89	PASS	PASS	1.52%
FFIRC - Fast internal reference frequency	MHz	ROOM	47.52	48.48	48.235	0.039	2.12	48.177	0.052	1.96	PASS	PASS	48.140	0.040	3.67	48.110	0.060	2.61	PASS	PASS	9.85%
IDD_ACTIVE - Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz VDD=5V	mA	ROOM	NA	12.50	10.149	0.074	10.52	10.135	0.107	7.35	NA	PASS	10.180	0.110	7.03	10.340	0.150	4.80	NA	PASS	0.25%
IDD_SLEEP - Sleep mode current, VDD=5V	mA	ROOM	NA	4.30	3.759	0.029	6.16	3.749	0.039	4.73	NA	PASS	3.750	0.040	4.58	3.770	0.032	5.52	NA	PASS	0.21%
IDD_DEEPSLEEP - Deepsleep mode current, VDD=5V SIRC=1, SXOSC=0	uA	ROOM	NA	115.00	103.500	1.668	2.30	103.959	1.556	2.37	NA	PASS	98.610	2.020	2.70	99.010	1.920	2.78	NA	PASS	4.25%
IDD_STANDBY - Standby mode current, VDD=5V SIRC enable, SXOSC disable	uA	ROOM	NA	16.00	4.493	0.188	20.38	5.060	0.122	29.95	NA	PASS	3.990	0.360	11.12	4.001	0.430	9.30	NA	PASS	3.14%
VIN - Analog input voltage VDD/2	V	ROOM	2.7335	2.7665	2.748	0.001	5.31	2.747	0.001	5.96	PASS	PASS	2.750	0.002	2.75	2.752	0.002	2.10	PASS	PASS	5.23%
ADC_channel_test VDD/2	V	ROOM	2.71	2.79	2.749	0.002	7.83	2.750	0.003	5.03	PASS	PASS	2.749	0.002	7.83	2.751	0.003	5.03	PASS	PASS	0.87%
RPU @5V-Internal pull-up resistors	kΩ	HOT	20.00	70.00	37.473	2.703	2.15	37.652	3.205	1.84	PASS	PASS	40.116	1.590	4.22	40.421	1.690	4.03	PASS	PASS	5.29%
RPD @5VInternal pull-down resistors	kΩ	HOT	20.00	70.00	34.116	2.615	1.80	34.467	2.248	2.15	PASS	PASS	36.089	1.620	3.31	36.319	1.320	4.12	PASS	PASS	3.95%
RPU @3.3V-Internal pull-up resistors	kΩ	HOT	20.00	100.00	75.857	1.431	5.62	74.135	1.108	7.78	PASS	PASS	78.782	1.887	1.98	79.081	2.082	1.75	PASS	PASS	3.66%
RPD @3.3VInternal pull-down resistors	kΩ	HOT	20.00	105.00	65.815	1.504	8.69	66.743	1.317	9.68	PASS	PASS	70.314	1.967	4.86	70.004	2.167	4.31	PASS	PASS	5.29%
PMC Bandgap Vref=1V	V	HOT	0.96	1.04	0.995	0.006	2.13	0.992	0.006	1.74	PASS	PASS	1.001	0.003	2.29	1.002	0.003	2.22	PASS	PASS	7.65%
FSIRC - Fast internal reference frequency	MHz	HOT	1.94	2.06	1.991	0.007	2.43	1.989	0.007	2.50	PASS	PASS	2.005	0.005	4.04	2.002	0.004	4.42	PASS	PASS	11.25%
FFIRC - Slow internal reference frequency	MHz	HOT	47.28	48.72	48.013	0.126	1.87	47.991	0.131	1.82	PASS	PASS	48.144	0.047	4.06	48.060	0.041	5.32	PASS	PASS	9.08%
IDD_ACTIVE - Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz VDD=5V	mA	HOT	NA	12.50	10.069	0.106	7.68	10.043	0.123	6.67	NA	PASS	10.050	0.120	6.81	10.110	0.195	4.08	NA	PASS	0.16%
IDD_SLEEP - Sleep mode current, VDD=5V	mA	HOT	NA	4.30	3.751	0.036	5.03	3.740	0.045	4.17	NA	PASS	3.724	0.040	4.80	3.777	0.046	3.82	NA	PASS	0.62%
IDD_DEEPSLEEP - Deepsleep mode current, VDD=5V SIRC=1, SXOSC=0	uA	HOT	NA	170.00	115.840	3.027	5.96	114.175	6.986	2.66	NA	PASS	126.200	4.820	3.03	125.900	3.750	3.92	NA	PASS	6.09%
IDD_STANDBY - Standby mode current, VDD=5V SIRC enable, SXOSC disable	uA	HOT	NA	50.00	13.876	2.189	5.50	12.142	3.428	3.68	NA	PASS	16.920	3.680	2.09	17.020	3.003	2.55	NA	PASS	6.09%
VIN - Analog input voltage	V	HOT	2.7250	2.7665	2.746	0.001	6.39	2.744	0.002	3.01	PASS	PASS	2.748	0.001	9.48	2.749	0.001	7.44	PASS	PASS	5.70%
ADC_channel_test VDD/2	V	HOT	2.71	2.79	2.749	0.002	7.79	2.747	0.002	5.04	PASS	PASS	2.748	0.002	7.79	2.747	0.002	5.04	PASS	PASS	1.86%
RPU @5V-Internal pull-up resistors	kΩ	COLD	20.00	70.00	29.991	1.255	2.65	29.339	1.047	2.97	PASS	PASS	25.439	0.965	1.88	25.590	0.946	1.97	PASS	PASS	9.10%
RPD @5VInternal pull-down resistors	kΩ	COLD	20.00	70.00	26.613	1.279	1.72	26.010	1.155	1.73	PASS	PASS	23.244	0.399	2.71	24.040	0.572	2.36	PASS	PASS	6.74%
RPU @3.3V-Internal pull-up resistors	kΩ	COLD	20.00	100.00	47.241	2.641	3.44	46.915	2.456	3.65	PASS	PASS	50.769	2.797	4.68	51.009	2.946	4.41	PASS	PASS	4.41%
RPD @3.3VInternal pull-down resistors	kΩ	COLD	20.00	105.00	41.497	2.476	2.89	42.103	2.248	3.28	PASS	PASS	45.770	2.988	3.43	45.980	2.857	3.61	PASS	PASS	5.03%
PMC Bandgap Vref=1V	V	COLD	0.96	1.04	1.001	0.007	1.80	0.998	0.006	1.95	PASS	PASS	1.002	0.002	5.81	1.001	0.002	5.49	PASS	PASS	1.24%
FSIRC - Slow internal reference frequency	MHz	COLD	1.94	2.06	2.003	0.010	1.88	1.999	0.008	2.61	PASS	PASS	2.006	0.005	2.47	2.008	0.005	2.97	PASS	PASS	3.01%
FFIRC - Fast internal reference frequency	MHz	COLD	47.28	48.72	48.205	0.063	2.73	48.121	0.079	2.52	PASS	PASS	48.192	0.107	2.00	48.196	0.108	2.10	PASS	PASS	0.89%
IDD_ACTIVE - Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz VDD=5V	mA	COLD	NA	12.50	10.195	0.085	9.04	10.180	0.121	6.39	NA	PASS	10.080	0.120	6.72	10.078	0.157	5.16	NA	PASS	0.92%
IDD_SLEEP - Sleep mode current, VDD=5V	mA	COLD	NA	4.30	3.789	0.033	5.23	3.769	0.043	4.08	NA	PASS	3.717	0.040	4.86	3.688	0.052	3.94	NA	PASS	1.67%
IDD_DEEPSLEEP - Deepsleep mode current, VDD=5V SIRC=1, SXOSC=0	uA	COLD	NA	115.00	99.997	2.166	2.31	101.013	2.122	2.20	NA	PASS	96.470	3.250	1.90	96.988	3.060	1.96	NA	PASS	3.07%
IDD_STANDBY - Standby mode current, VDD=5V SIRC enable, SXOSC disable	uA	COLD	NA	16.00	4.248	0.121	32.50	4.961	0.273	13.49	NA	PASS	3.832	1.100	3.69	4.028	1.010	3.95	NA	PASS	2.60%
VIN - Analog input voltage VDD/2	V	COLD	2.73	2.77	2.746	0.001	3.76	2.748	0.002	3.01	PASS	PASS	2.748	0.001	4.83	2.749	0.001	4.26	PASS	PASS	7.17%
ADC_channel_test VDD/2	V	COLD	2.71	2.79	2.749	0.002	7.34	2.746	0.003	4.02	PASS	PASS	2.748	0.002	7.34	2.748	0.003	4.02	PASS	PASS	1.63%

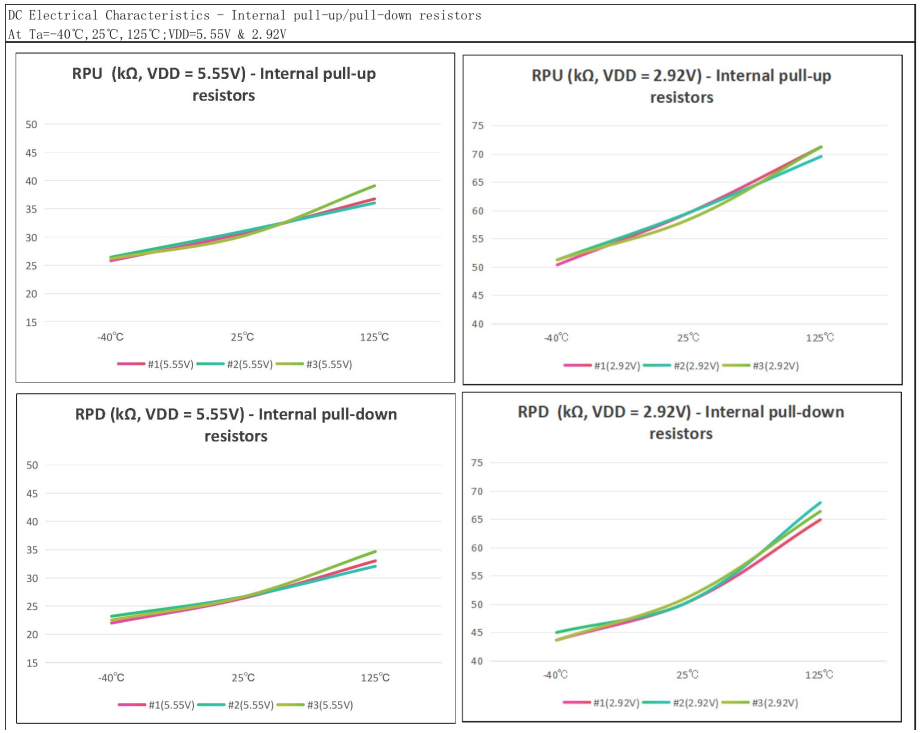
Validation Conclusion:

- HTOL 0 Fail, ED result is PASS.
- Compared with the average value of HTOL test parameters before revision, there is no abnormality.

ZVEI Supplementary Reliability Validation -- E7

Validation Plan:

- Characteristic test data related to the revision.

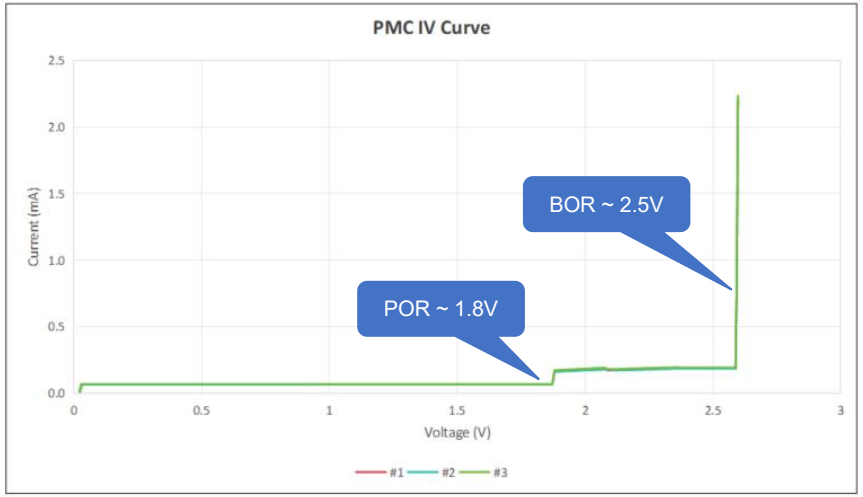


IO RPU & RPD are consistent with those of the EVB

Validation Conclusion:

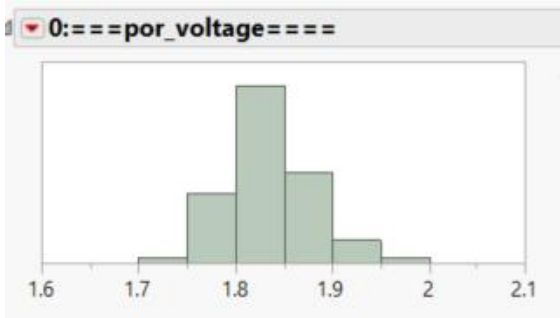
- The characteristic test data related to the revision is consistent with the board-level verification data and meets the Datasheet requirements.

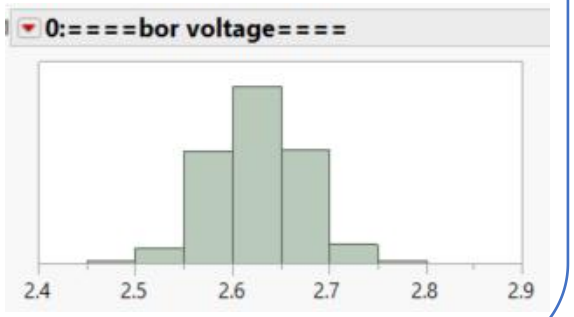
2.3.1. PMC IV Curve



在 25℃，Typical CZ PMC IV Curve 显示 POR 电压约 1.8V

Based on the data of 1000 samples, the POR/BOR distribution meets the expectations and is consistent with the board-level verification.





02-3 Hardware Revision Validation Report_Trial Run Report

改版前后测试结果对比

Comparison of Test Results Before and After Revision:

测试站点	改版后批次良率	改版前量产批次良率
CP1/2(HHG)	98.67%	98.50%
CP ROOM	97.68%	97.95%
CP HOT	99.57%	99.43%
CP COLD	99.67%	98.91%
Total Yield:	95.65%	94.89%

The CP yield of the revised batch is consistent with that of the mass-produced batch before revision, with no abnormalities.

Comparison of CP Three-Temperature Test Yield:

	测试项	测试站点	改版后批次失效率	改版前量产批次失效率
Top1	BIN16_SCAN_stuck	CP ROOM	1.27%	1.25%
Top2	BIN22_SCAN_iddq	CP ROOM	0.33%	0.32%
Top3	Bin26_mbist_test	CP ROOM	0.31%	0.31%
Top4	BIN20_firc_freq_check_5v5	CP HOT	0.22%	0.22%
Top5	BIN19_SCAN_transition	CP ROOM	0.17%	0.15%

The main failed test items and failure rates of the revised batch are consistent with those of the mass-produced batch before revision, with no abnormalities.

Validation Conclusion:

- The CP three-temperature test yield and CP three-temperature test Fail BIN rate are consistent before and after the revision, with no abnormalities.

云途 YUNTU

THANKS

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