YTM32B1LE0x Data Sheet

Support: YTM32B1LE05H0MLHT, YTM32B1LE05H0MLFT, YTM32B1LE05H0MLET, YTM32B1LE05H0MFMR, YTM32B1LE05H0MFMIR, YTM32B1LE04H0MLFT, YTM32B1LE04H0MLET, YTM32B1LE04H0MFMR

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1 Features

- AEC-Q100 qualified
- ASIL-B compliant
- RoHS compliant
- ARM Cortex-M0+
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single-cycle access to I/O: Up to 50 percent faster than standard I/O, improves reaction time to external events allowing bit manipulation and software protocol emulation
  - Two-stage pipeline: Reduced number of cycles per instruction (CPI), enabling faster branch instruction and ISR entry, and reducing power consumption
  - Excellent code density in comparison to 8-bit and 16-bit MCUs: Reduced flash size, system cost and power consumption
  - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools
  - Simplified architecture: 56 instructions and 17 registers enable easy programming and efficient packaging of 8/16/32-bit data in memory
  - Linear 4 GB address space removes the need for paging/banking, reducing software complexity
  - ARM third-party ecosystem support: Software and tools to help minimize development time/cost
  - Support systick with a 8-bit divider and enablement
- 4 DMA channels with up to 41 peripheral hardware trigger sources
- DIVSQRT module with 32-bit integer divide and square root arithmetic operations
- Memory
  - Up to 128 KB Program Flash (PFlash) with ECC
  - Up to 16 KB SRAM with ECC
  - Single power supply (2.97 ~ 5.5 V) with full functional flash program/erase/read operations
- Clocks
  - Fast IRC (FIRC), up to 48 MHz
  - Fast crystal oscillator (FXOSC), range 4~40 MHz
  - Slow IRC (SIRC), up to 2 MHz
  - Slow crystal oscillator (SXOSC), run at 32.768 KHz
  - Low power oscillator (LPO), run at 750 Hz
- Power Management
  - Low-power ARM Cortex-M0+ with excellent energy efficiency
  - Support four power modes: Active, Sleep, Deepsleep and Standby
  - Support clock gating for unused modules
  - Support specific peripherals remain working in low power modes
- Mixed-signal Analog
  - One Analog-to-Digital Converter (ADC) with 12-bit 1Msps sample rate, it has 16 channels and supports temperature sensor
  - One Analog Comparator (ACMP) with 8-bit DAC
- Communications
  - Up to three Universal Asynchronous Receiver Transmitter (UART) with optional 13-bit break, full duplex Non-return to Zero (NRZ) and LIN extension support
  - Up to three Serial Port Interface (SPI) with full-duplex or single-wire bidirectional and master or slave mode
  - Up to two Inter-integrated Circuit (I2C)
  - One FlexCAN support CAN2.0A/B and FD
- Reliability, Safety and Security
  - Clock Monitor Unit (CMU)
  - Internal Watchdog (WDG) with independent clock source
  - Cyclic Redundancy Check (CRC) with 32/16/4-bit polynomial generator
- Timers
  - Up to three Enhanced Timers (eTMR)
  - Periodic Timer (pTMR) for RTOS task scheduler time base for timer modules
  - Low Power Timer (lpTMR)
  - 16-bit Real Time Clock (RTC)
- Human-Machine Interface
  - Up to 58 GPIO pins with interrupt functionality
  - Non-Maskable Interrupt (NMI)
- I/O and package
  - Support LQFP 64/48/32
  - Support QFN 32
- Operating Characteristics
  - Voltage range: 2.97V ~ 5.5V
  - Ambient temperature range: -40°C ~ 125°C

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2 Overview

YTM32B1LE0x series provide the highly scalable portfolio of ARM® Cortex®-M0+ MCUs in the automotive industry. With 2.97 ~ 5.5 V supply and focus on exceptional EMC/ESD robustness, YTM32B1LE0x series devices are well suited to a wide range of applications in electrical harsh environments, and is optimized for cost-sensitive applications offering low pin count option. The YTM32B1LE0x series offers a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32B1LE0x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

3 Block Diagram

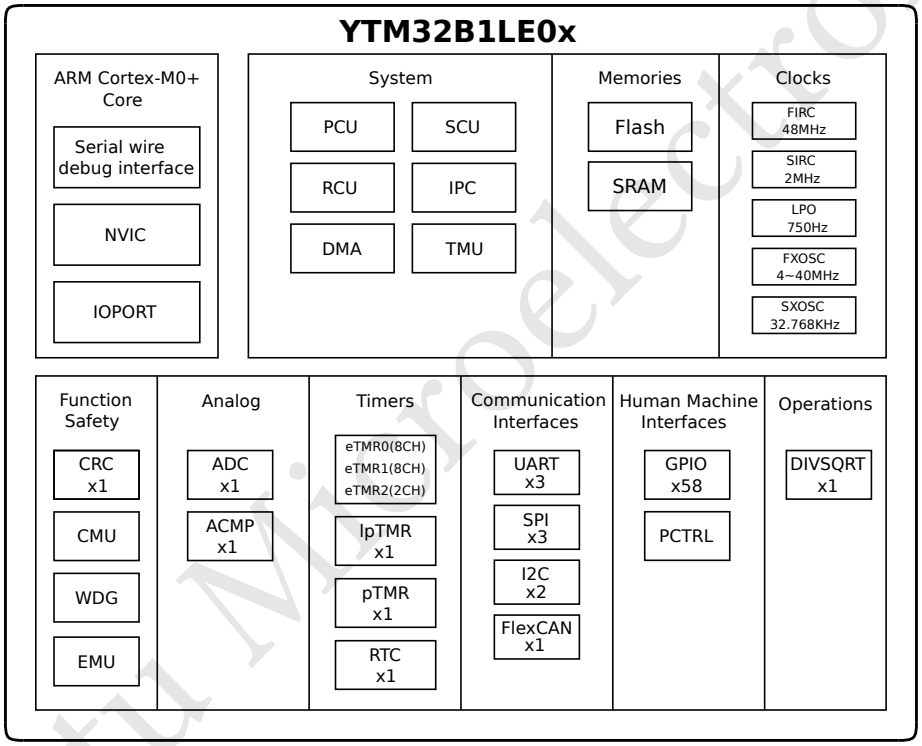

Figure 1: YTM32B1LE0x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1LE0x device.

4.1 Core Modules

4.1.1 ARM Cortex-M0+

- Up to 48 MHz core frequency from 2.97 V to 5.5 V
- Supports up to 32 interrupt request sources

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- 2 stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiplier

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Supports four priority levels for interrupts with two bits in each IPRn registers
- Includes a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast internal RC oscillator (FIRC)
  - Up to 48 MHz
  - Default system boot clock source
  - Support trim for temperature and process
- Slow internal RC oscillator (SIRC)
  - Run at 2 MHz
  - Can be selected as system clock source
  - Always on unless it is forced to be disable in standby mode
  - Support trim for temperature and process
- Fast crystal oscillator (FXOSC)
  - Support 4~40 MHz crystal
  - Can be selected as system clock source
  - Support bypass mode
- Slow crystal oscillator (SXOSC)
  - 32.768 KHz real time oscillator
  - Can't be selected as system clock
  - Provides accurate clock to watchdog(WDG) and real time clock(RTC)
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock
- SCU contains 2 CMU blocks
  - CMU monitors FXOSC and FIRC clock
  - CMU reference clock is SIRC
  - CMU can detect frequency out of range, loss of checked clock and loss of reference clock

4.2.2 Power Control Unit (PCU)

- Combination of power management blocks including POR, Bandgap, LVD, Brownout, full power regulator and low power regulator
- Responsible for sequencing the system enter and exit the Standby mode
- Low Voltage Reset(LVR) for all system relevant power domains

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4.2.3 Reset Control Unit (RCU)

- Manage the system power up, pin reset, functional reset and fault reset flow
- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work in Active, Sleep, Deepsleep and Standby mode

4.2.4 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection as follow
  - FIRC 48 MHz
  - FXOSC 4~40 MHz
  - SIRC 2 MHz
  - SXOSC 32.768 KHz
  - LPO 750 Hz
- IPC clock divide values from 1 to 16

4.2.5 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
  - Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/not change selectable
- Up to 4 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware trigger
- Up to 41 peripheral hardware triggers
- Internal data fifo for data transfer
- Support update DMA transfer information from system memory after transfer complete

4.2.6 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- ADC/ACMP trigger synchronize selection
- Software trigger generate
- eTMR external clock and fault selection
- eTMR channel input/output selection
- Chip and die information

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- 128 KB Program Flash(PFlash) with ECC which supports single error correction (SEC) and double error detection (DED)

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- 24 MHz single cycle reads of bytes, aligned halfword (16-bit) and aligned word (32-bit)
- Automated generation of ECC parity while programming and erasing
- Optional interrupt on command completion
- Program and erase operations do not require any special power sources other than the normal VDD supply

4.3.2 On-chip SRAM

- 16 KB SRAM with ECC supports single error correction (SEC) and double error detection (DED)

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 1.0μs for 12-bit resolution conversion time
- Support DMA and conversion result FIFO with watermark
- Support up to 17 input channels
  - 16 channels to measure external analog signals from pad
  - 1 channel to measure internal temperature sensor
- Support multiple conversion modes
  - Single mode: convert one or more channels once a time
  - Continuous mode: convert one or more channels until stopped by software
  - Discontinuous mode: convert one channel once a time
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
- Support work and wake up when the whole chip under low power mode

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-shot mode

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    - Loop mode
- Up to 8 channels can be used to execute automatic comparisons
- Digitally filtered, filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in low power mode
- Support independent DAC input channel to the comparator
  - Optional DAC reference source: internal or external reference source
  - 8-bit DAC resolution
- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
    - Generate interrupt when the comparison results don't match expectations
- Interrupt can generate without any clock
- A comparison event can be selected to trigger DMA transfer

4.5 Timer

4.5.1 Periodic Timer (pTMR)

- Timers can generate interrupts
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timers to a longer timer

4.5.2 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wake-up from any low power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler and glitch filter
- Configurable input source for pulse counter
  - Rising-edge
  - Falling-edge
- Support triggering DMA transfer

4.5.3 Enhanced Timer (eTMR)

- There are three eTMRs with below configurations
  - eTMR0: 8 channels
  - eTMR1: 8 channels
  - eTMR2: 2 channels
- Bus clock and external clock can be the source clock of each eTMR
- Each eTMR contains a 7-bits clock prescaler
- Each eTMR contains a 16-bit counter
- Each channel can be configured as three modes
  - Input Capture mode
    - Support rising edges, falling edges or dual edges

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    - Support input filter with a prescaler that can be selected for channels, eTMR0: channel 0-3, eTMR1: channel 0-3, eTMR2: channel 0-1
  - Output Compare mode
    - The output signal can be configured to set, clear or toggle on match point
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair channels: Pair channels: channel 0-1, channel 2-3, channel 4-5, channel 6-7
    - Supports independent deadtime insertion for odd and even channel
    - Fault control mechanism: eTMR0 and eTMR1 support 4 fault inputs for global fault control
- Each eTMR can be configured to generate triggers
  - Output triggers on match point
  - Output pulse-out with adjustable pulse width
- PWM outputs can be controlled by software
- Polarity control is available for every channel of each eTMR
- Mask control is available for every channel of each eTMR
- Synchronized loading of write buffered registers is available in each eTMR
- Capture test mode is available in each eTMR
- eTMR1 can be configured as quadrature decoder, which supports relative position counting or external event counting
  - Support phase A and phase B input filters
  - Contains a independent 16-bits counter with a clock prescaler
  - Support 4 up-down counting modes
- Support GTB (Global Time Base) for all eTMRs
- Support several interrupts
  - Channel interrupt (input capture interrupt and output compare interrupt)
  - Counter overflow interrupt
  - Fault interrupt
- Support DMA

4.5.4 Real Time Clock (RTC)

- 32-bit seconds counter with prescaler of 1 Hz
- Support compensation with RTC clock
- Lock support of register access for control and alarm register
- Selectable of 1 Hz to 128 Hz square wave output
- Support two clock sources

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit uses
  - CRC-32 polynomial:
    $X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - CRC-16 polynomial: $X^{16} + X^{12} + X^5 + 1$
  - CRC-4 polynomial: $X^4 + X + 1$
- Programmable initial seed value
- Accept with 8-bit or 16-bit or 32-bit input data size
- Option to transpose input data or output data (the CRC result) bitwise
- Option for inversion of final CRC result

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- 32-bit CPU register programming interface

4.6.2 Watchdog (WDG)

- Support regular or window servicing mode
- Support reset request or interrupt for first timeout
- Support fixed key for dog feeding

4.6.3 ECC Management Unit (EMU)

- Error injection
  - Error injection provides a method for diagnostic coverage of SRAM.
  - Error injection uses two-stage enable mechanism.
  - Error injection provides support for inducing single-bit or multi-bit inversions on read data when accessing SRAM
- Error reports
  - Error report provides information and optionally interrupt notification on SRAM error events associated with ECC (Error Correction Code) and parity
  - Error report provides count registers which count all correctable error so far

4.7 Operation Unit

4.7.1 Divide and Square Root (DIVSQRT)

- Support 32-bit integer divide and square root arithmetic operations
  - Divide arithmetic support unsigned and signed 32-bit integer
  - Support selectable action to divide-zero
  - Square arithmetic support unsigned 32-bit integer
- Input data and result are memory-mapped with easy programming model
  - Support data write to start calculation and data read get result
  - Support control and status register for calculation

4.8 Communication Interfaces

4.8.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0 Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32 or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 32 message buffers of 8 bytes data length each, configurable as Rx or Tx

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- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8-bit) IDs, with up to 32 ID Filter Table elements

4.8.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN mode
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baud rate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wake-up
- Support transmit/receive line switch, single line mode
- Hardware flow control support

4.8.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support Master and slave mode
- Support Transmit/Receive via DMA

4.8.4 Inter-Integrated Circuit (I2C)

- Support standard, fast and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave

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- Support SMBUS mode
- Support multi-master arbitration and synchronization
- Support Master and slave clock stretching
- Transmit/Receive FIFO (Master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA
- I2C1 do not support slave mode

4.9 Human Machine Interface

4.9.1 General Purpose Input/Output (GPIO)

- Port Data Input register visible in all digital pin multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Port Input Disable register
- Pin interrupts
  - Interrupt flag and enable registers for each pin, functional in all digital pin multiplexing modes
  - Support for interrupt, DMA request or Peripheral Trigger configured per pin
  - Support for edge sensitive (rising, falling, both) or level sensitive (low, high) configured per pin
  - Asynchronous wake-up in low power modes
  - Each pin can be configured for 1 of interrupt, DMA request or trigger output

4.9.2 Port Controller (PCTRL)

- Individual pull control fields with pull-up, pulldown and pull-disable support
- Individual drive strength field supporting high and low drive strength
- Individual mux control field supporting analog or pin disabled, GPIO and up to 6 chip-specific digital functions
- Individual passive filter field supporting enabling and disabling passive filter for specific input

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Information

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash(KB)	SRAM(KB)	Pin count	Package	GPIOs (Normal)	ADC channels	FlexCAN
YTM32B1LE05H0MLHT	128KB	16KB	64	LQFP	58	16	1
YTM32B1LE05H0MLFT	128KB	16KB	48	LQFP	43	13	1
YTM32B1LE05H0MLET	128KB	16KB	32	LQFP	28	12	1
YTM32B1LE05H0MFMR	128KB	16KB	32	QFN	28	9	1
YTM32B1LE05H0MFMIR	128KB	16KB	32	QFN	28	9	1
YTM32B1LE04H0MLFT	64KB	8KB	48	LQFP	43	13	1
YTM32B1LE04H0MLET	64KB	8KB	32	LQFP	28	12	1
YTM32B1LE04H0MFMR	64KB	8KB	32	QFN	28	9	1

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5.1 Part Number Information

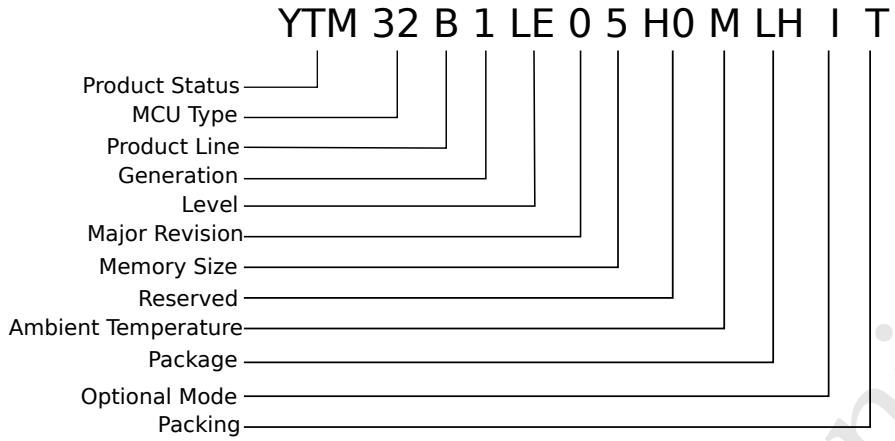

Figure 2: Part Numbers Field

The part numbers field description is shown as below.

Table 2: Part Number Field Description

Field	Description	Values					
YTM	Product Status	YTM: Qualified PTM: Prototype					
32	MCU Type	32: 32-bit					
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network Z: High voltage, integrity					
1	Generation	1st generation product					
Lx	Level	Hx: High end Mx: Middle end Lx: Low end					
0	Major Revision	1st revision					
5	Memory Size		1	2	3	4	5
		H	2M	4M	6M	8M	-
		M	64K	128K	256K	512K	1M
		L	8K	16K	32K	64K	128K
H0	Reserved	Reserved					
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C					
		Pin Counts	LQFP	QFN	BGA	-	-
		32	LE	FM	-	-	-
		48	LF	-	-	-	-

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Table 2: Part Number Field Description

Field	Description	Values					
LH	Package	64	LH	-	-	-	-
		100	LL	-	MH	-	-
		144	LQ	-	-	-	-
		176	LU	-	-	-	-
		257	-	-	MM	-	-
		289	-	-	MQ	-	-
I	Optional Mode	I: ISELED					
T[1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark will not contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	135	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Typ.	Max.	Notes
MSL	Moisture sensitivity level	–	3	–	1

NOTE:

- Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- Storage conditions are formulated in accordance with MSL3 standards. For specific requirements, refer to the instructions on the aluminum foil packaging bag. Chip storage shall meet the following: temperature < 40°C, humidity < 90% RH, storage period 24 months.

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2

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Table 5 continued from previous page

Symbol	Description	Min.	Max.	Unit	Notes
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8[1]	V	
I_{VDD}	Maximum current into V_{DD}	–	70	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.
10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	V_{DD}	V	
V_{REFH}	Reference voltage	2.97	V_{DDA}	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-1	1	mA	

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Table 7 continued from previous page

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	–	15	mA	
T_{ramp}	MCU supply ramp rate	5 V/100ms	100 V/ms	–	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} − 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}-0.3V-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}-(V_{DD}+0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.1 * V_{DD}	–	0.3 * V_{DD}	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	5	10	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	5	10	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	12	20	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	12	20	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	50	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	–	500	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	V_{DD}	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	V_{SS}	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	0.002	0.5	μA	

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Table 8 continued from previous page

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
	High Drive pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.1 * V_{DD}	–	0.3 * V_{DD}	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	10	20	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	10	20	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	20	30	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	20	30	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	380	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	–	500	nA	
V_{OH}	Output high voltage					
	Normal drive pad (4V $\leq$ V_{DD} $\leq$ 5.5V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	V_{DD}	V	
V_{OL}	Output low voltage					
	Normal drive pad (4V $\leq$ V_{DD} $\leq$ 5.5V, I_{OL} = -2.8mA)	V_{SS}	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	0.002	0.5	μA	
	High drive pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	15	–	70	kΩ	

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6.2.5 Power and Ground Pins

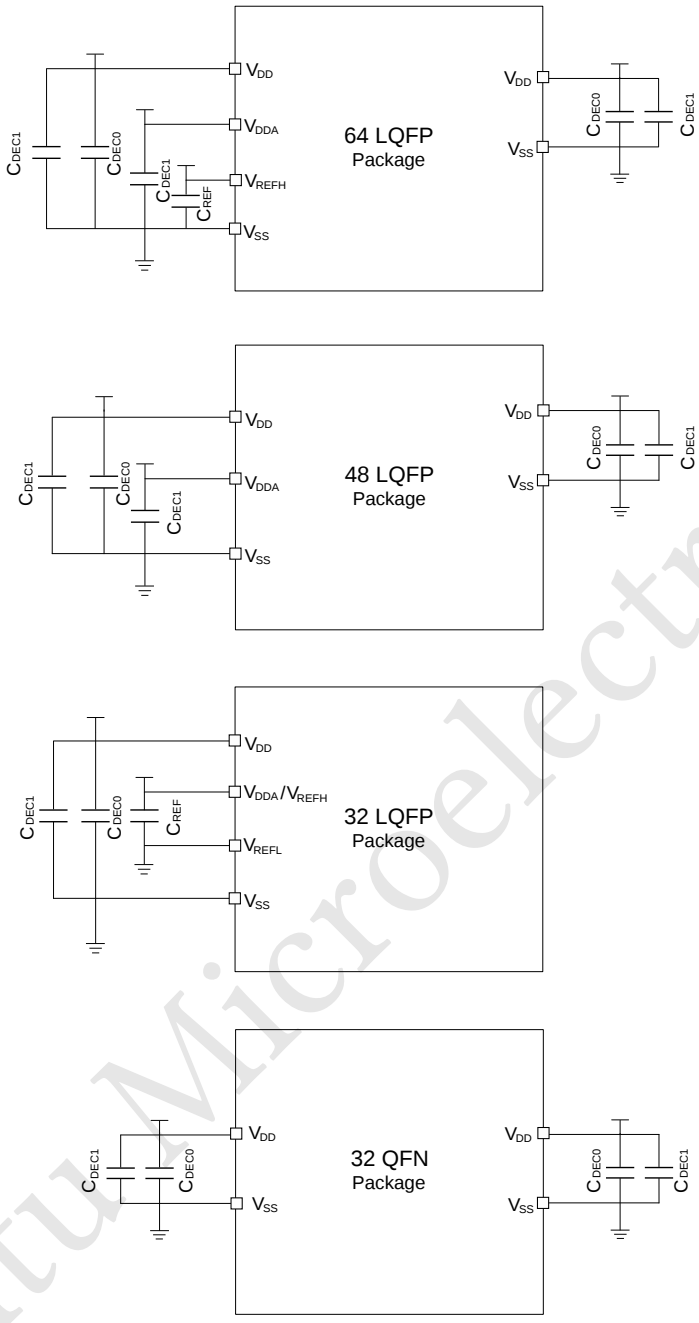

Figure 3: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1,2,3]	ADC reference high decoupling capacitance	50	100	200	nF
C_{DEC0}[2,3,4]	Recommended decoupling capacitance for V_{DD}	1	2.2	10	μF
C_{DEC1}[2,3,4]	Recommended bypass decoupling capacitance for V_{DD}	50	100	200	nF

1. For improved performance, it is recommended to use 2.2 μF, 0.1 μF and 1nF capacitors in parallel.

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2. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
3. All decoupling capacitors must be low ESR ceramic capacitors(for example X7R type).
4. The requirement and value of C_{DEC} will be decided by the device application requirement.

6.2.6 POR, LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BOR}	Rising and falling V_{DD} BOR detect voltage	2.3	2.5	2.7	V	
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.5	1.8	2.1	V	
V_{LVD}	Falling low-voltage threshold(LVDCFG=4)	2.5	2.6	2.7	V	
	Falling low-voltage threshold(LVDCFG=10)	3.8	4.2	4.5	V	
V_{LVD_HYST}	LVD hysteresis(LVD5VHYS=01b)	-2	–	2	%	
	LVD hysteresis(LVD5VHYS=10b)	-4.2	–	4.2	%	
	LVD hysteresis(LVD5VHYS=11b)	-8.4	–	8.4	%	
V_{bg}	Bandgap voltage reference	0.96	1.0	1.04	V	
V_{DD15}	MCU VDD15 LDO output voltage	1.35	1.5	1.65	V	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	1μs	–
DEEPSLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	5μs	–
STANDBY -> ACTIVE	FIRC	48MHz, 24MHz	–	40μs	–
T_{POR}	FIRC(reset value)	48MHz, 24MHz	–	250μs	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	FIRC	Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	$\leq$ 25 °C	–	9.0	14.5	mA
				125 °C	–	9.0	14.5	mA
SLEEP	I_{DD_SLEEP}	–	Sleep mode current, V_{DD}=5V	$\leq$ 25 °C	–	3.9	5.0	mA
				125 °C	–	4.0	5.0	mA
DEEPSLEEP	$I_{DD_DEEPSLEEP}$	FIRC	Deepsleep mode current, V_{DD}=5V SIRC=1, SXOSC=0	$\leq$ 25 °C	–	100	150	μA
				125 °C	–	130	250	μA
STANDBY	$I_{DD_STANDBY}$	FIRC	Standby mode current, V_{DD}=5V SIRC=0, SXOSC=0	$\leq$ 25 °C	–	4.0	20	μA
				125 °C	–	50	100	μA

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6.2.9 Power Sequence

6.2.9.1 Power Up Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

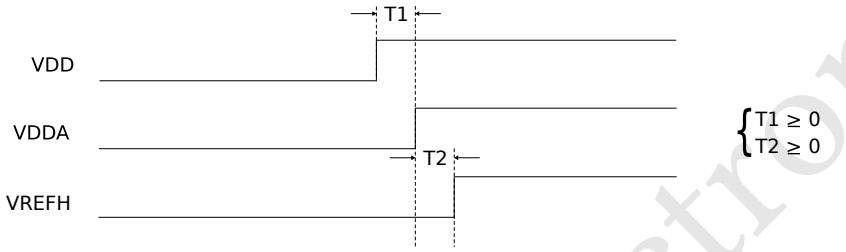

Figure 4: Power Sequence

6.2.9.2 MCU Power Supply Ramp Rate

During the power-up sequence of MCU, it is critical that the power supply maintains a ramp-rate within the specified range, starting from V_{DD_OFF} at 0.1V and rising to the MCU's operational voltage level (V_{DD}). Failure to comply with this specification may result in unintended behavior, operational stagnation or even damage to the MCU.

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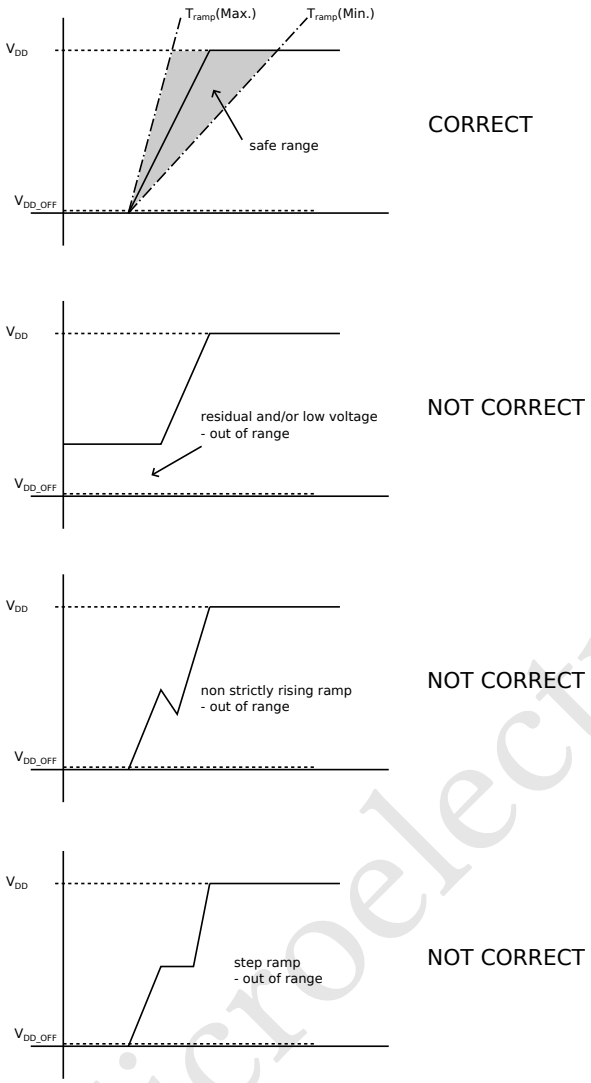

Figure 5: Power Supply Ramp Rate

6.2.9.3 Power Up Requirements

It is necessary to ensure that VDD meets the following timing during the power-up process of YTM32B1LE0x.

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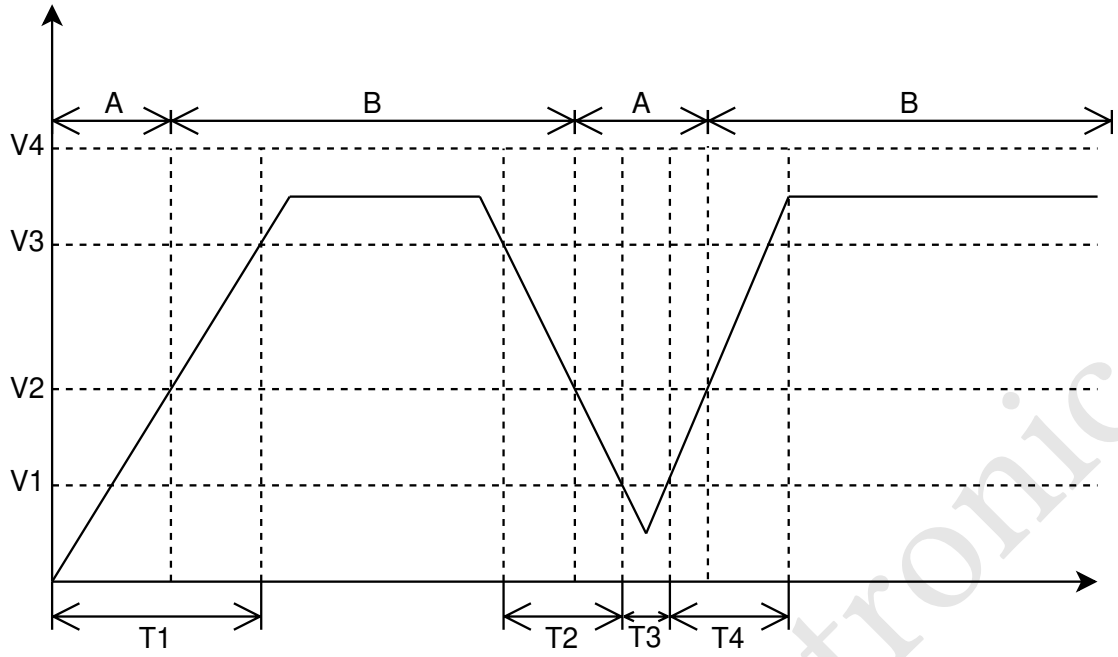

A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 6: Power Up Requirements

Symbol	Name	Description	Unit (V)
V1	Restart threshold voltage	When restarting the MCU, VDD should keep below V1 for a period of T3.	0.2
V2	Minimum MCU operating voltage	The MCU starts working when the power supply reaches V2.	2.5
V3	Lower voltage limit of MCU operating normally	Minimum operating voltage for normal MCU operation and interaction with peripherals.	2.97
V4	Upper voltage limit of MCU operating normally	Maximum operating voltage for normal MCU operation and interaction with peripherals	5.5

Symbol	Name	Description	Requirement
T1	Power up time	Rising time of MCU VDD from 0V to V3	10 μs $<$ T1 $<$ 50ms
T2	Power down time	Drop time of MCU VDD from V3 to V1 during the MCU restart/power down process	10 μs $<$ T2 $<$ 500ms
T3	Restart threshold voltage retain time	Minimum duration of MCU VDD below V1, when restarting MCU	T3 $>$ 100 μs
T4	Restart power up time	Rising time of MCU VDD normal operation from V1 to V3	10 μs $<$ T4 $<$ 50ms

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NOTE: The power-up process needs to be restarted if a VDD voltage drop occurs during the T1~T4 power-up process before the VDD voltage reaches the V2 voltage. Restarting the power-up of MCU needs to ensure that the voltage of VDD continues to drop below V1 and remains there for T3 time.

6.2.10 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Power Supply Fluctuation Requirements

1. The power supply fluctuation must be maintained within ± 10% of the power supply voltage, and the fluctuation frequency should not exceed 100 KHz.
2. The maximum power supply fluctuation should not exceed ± 20% of the power supply voltage, and in this case, the fluctuation frequency should be less than 30 KHz.
3. Power supply fluctuations exceeding the above requirements may cause chip abnormalities and require a power-up process according to the requirements outlined in Power Up Requirements.

6.3.2 Device Clock Specifications

Symbol	Description	Min.	Max.	Unit	Notes
f_{core}	System and core clock	–	48	MHz	
f_{bus}	Bus clock	–	24	MHz	

6.3.3 I/O Electrical Characteristics

6.3.3.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

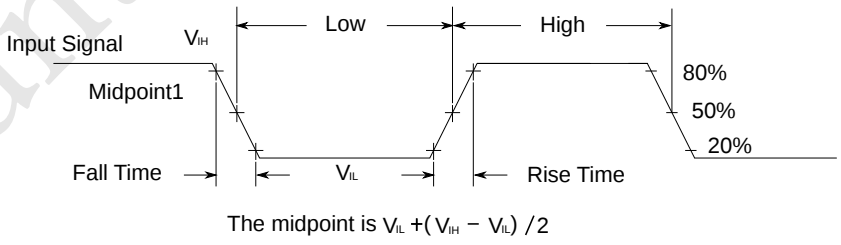

Figure 7: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads

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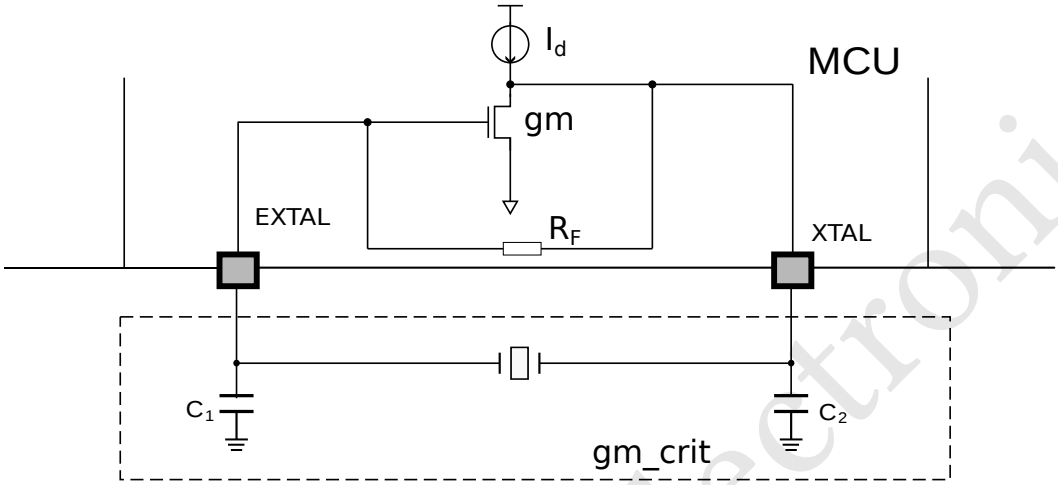
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40MHz) Characteristics

The following diagram is Fast Crystal OSC circuit.



- The internal circuitry of the chip utilizes an I_d current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (gm) of the amplifying transistor is greater than the intrinsic gain (gm_crit) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that gm>5*gm_crit.
- R_F provides the DC bias point for the input terminal of the amplifying transistor.

Figure 8: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	–	5.5	V	
I_{DDOSC}	FXOSC oscillator	–	2.0	–	mA	
F_{OSC}	Oscillator frequency	4	–	40	MHz	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, V_{DD}=5V	0.7*V_{DD}	–	V_{DD}	V	
	Input high voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	0.7*V_{DD}	–	V_{DD}	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, V_{DD}=5V	V_{SS}	–	0.3*V_{DD}	V	
	Input low voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	V_{SS}	–	0.3*V_{DD}	V	
$T_{FXOSCSU}$	FXOSC startup time (40MHz oscillator)	–	0.5	3.5	ms	
D_{FXOSC}	Duty of FXOSC (40MHz oscillator)	40	50	60	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC internal feedback resistor	400	500	700	kΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (40MHz oscillator)	1.2	2.25	V_{DD}	V	

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1. Crystal oscillator circuit provides stable oscillations when gm > 5 * gm_crit. The gm_crit is defined as: gm_crit=4 * (ESR + R_S) * $(2\pi F)^2$ * $(C_0 + C_L)^2$

where:

- gm is the transcondutance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [\ C_1 * C_2 / (C_1 + C_2)\ ]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins.

Table 18: Startup Time - Gain Selection for gm of 40MHz Crystal Oscillator Circuits (Simulation)

Gain Setting	gm (at startup)			Unit
	Min.	Typ.	Max.	
0			0	mS
1	1.4	2.2	3.6	mS
2	2.8	4.5	7.2	mS
3	4.2	6.8	10.8	mS
4	4.9	7.9	12.6	mS
5	6.2	10.2	16.2	mS
6	7.6	12.5	19.9	mS
7	9.1	14.7	23.5	mS

6.4.2 FIRC(48MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	48	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-1.0	–	1.0	%	
	FIRC frequence accuracy, factory trimmed, -40°C – 125°C	-1.5	–	1.5	%	
I_{FIRC}	FIRC operating current	–	250	–	μA	
$T_{Startup}$	Startup time	–	–	20	μs	

NOTE:

- For CAN communication, high-precision clock sources (e.g., FXOSC, PLL) must be used to comply with ISO 11898-1 standard; FIRC is not recommended for direct use as the PE clock of FlexCAN.
- For LIN/UART communication, it is recommended to use high-precision clock sources (e.g., FXOSC, PLL); if FIRC is used, evaluation must be conducted on frequency differences between chips, temperature effects, and frequency deviations of other devices in LIN/UART network.

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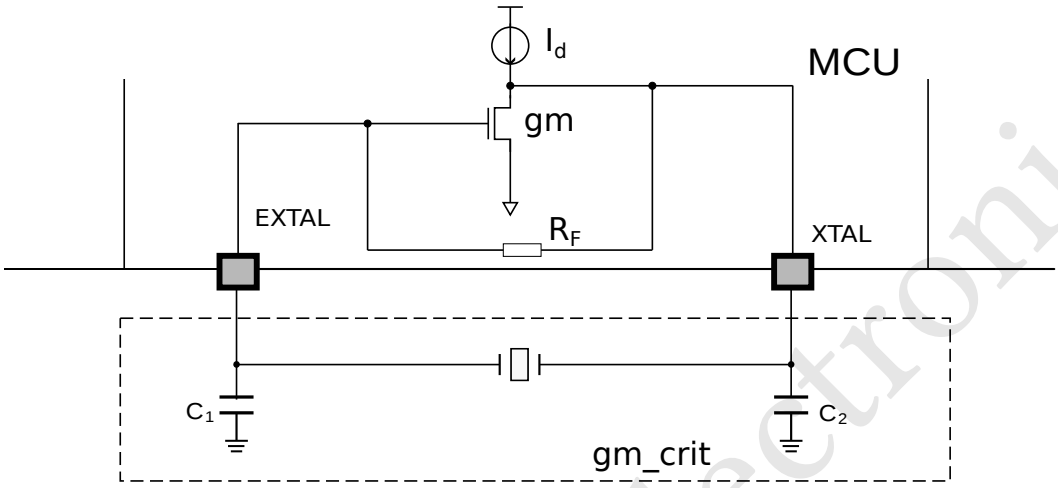
- For applications with high requirements on the absolute frequency of the clock (e.g., PWM output, timing tasks), evaluation must be conducted on frequency differences between FIRC and SIRC among different chips and their temperature effects.

6.4.3 SXOSC(32.768KHz) Characteristics

The following diagram is SXOSC circuit.



- The internal circuitry of the chip utilizes an I_d current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (gm) of the amplifying transistor is greater than the intrinsic gain (gm_crit) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that gm>5*gm_crit.
- R_F provides the DC bias point for the input terminal of the amplifying transistor.

Figure 9: SXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SXOSC}	Slow crystal oscillator frequency	30	32.768	35	KHz	
I_{DDOSC}	SXOSC oscillator	–	4	–	μA	
$T_{startup}$	SXOSC startup time (32.768KHz oscillator)	–	–	1	s	
D_{SXOSC}	Duty of SXOSC (32.768KHz oscillator)	40	50	60	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	SXOSC internal feedback resistor	6	8	11	MΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (32.768KHz oscillator)	0.94	1.2	V_{DD}	V	

1. Crystal oscillator circuit provides stable oscillations when gm > 5 * gm_crit. The gm_crit is defined as: $gm_crit=4 * (ESR + R_S) * (2\pi F)^2 * (C_0 + C_L)^2$

where:

- gm is the transcondutance of the internal oscillator circuit. gm > 10 μS
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation

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- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [C_1 * C_2 / (C_1 + C_2)]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins

6.4.4 SIRC(2MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	2	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-3.0	–	3.0	%	
	SIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-4.0	–	4.0	%	
	SIRC frequence accuracy, factory trimmed, −40 °C – 125 °C	-5.0	–	5.0	%	
I_{SIRC}	SIRC operating current	–	23	–	μA	
$T_{Startup}$	Startup time	–	10	50	μs	

NOTE:

- For CAN communication, high-precision clock sources (e.g., FXOSC, PLL) must be used to comply with ISO 11898-1 standard; FIRC is not recommended for direct use as the PE clock of FlexCAN.
- For LIN/UART communication, it is recommended to use high-precision clock sources (e.g., FXOSC, PLL); if FIRC is used, evaluation must be conducted on frequency differences between chips, temperature effects, and frequency deviations of other devices in LIN/UART network.
- For applications with high requirements on the absolute frequency of the clock (e.g., PWM output, timing tasks), evaluation must be conducted on frequency differences between FIRC and SIRC among different chips and their temperature effects.

6.4.5 LPO(750Hz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{LPO}	Low power oscillator frequency	300	750	2000	Hz	

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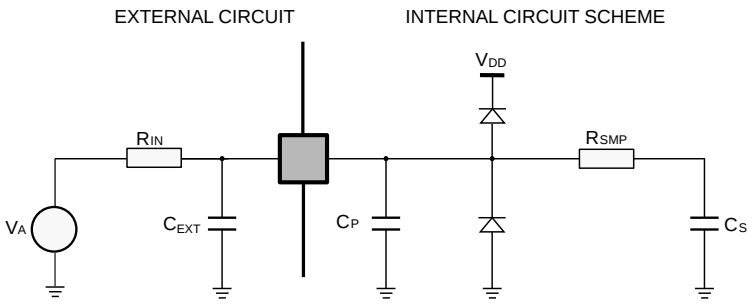
6.4.6 ADC Characteristics



Note: R_{IN} is the internal resistance of signal source.

Figure 10: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	
I_{VDDA}	Analog supply current		–	2	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		0	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	–	800	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		–	–	1.5	kΩ	
C_{EXT}	External capacitance		50	–	–	nF	
C_P	Pin capacitance		–	6	–	pF	
C_S	Sampling capacitance		–	6	7	pF	

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		5	–	–	μs	
T_{SAMPLE}	Sampling time		200	–	2000	ns	
T_{sample_TS}	Tempsensor sampling time	–	500	–	2000	ns	

1. These parameters of this table can be configured by register, please refer to Reference Manual for details.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
DNL	Differential nonlinear	12-bit resolution	–	±1.0	–	LSB	
INL	Integer nonlinear	12-bit resolution	–	±2.0	–	LSB	

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Table 25 continued from previous page

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
ACC_{TS}	Temperature sensor accuracy		-10		10	°C	
K[1]	Slope of temperature and voltage curve	ADC sampling frequncy @ 500kHz		616.9		°C / V	
F_{ADC}	ADC conversion clock		2		16	MHz	2

1. T = C - K*V, see Reference Manual for details.
2. ADC conversion clock = ADC function clock / [(ipc_divider +1) * (adc_clock_div +1)]

6.4.7 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		2.97	5.0	5.5	V	
I_{ACMP}	Analog supply current		–	20	40	μA	
$V_{INOFFSET}$	Analog input offset voltage		-10	–	10	mV	
V_{IN}	Analog input voltage		V_{SS}	–	V_{DD}	V	
V_{HYST0}	Analog comparator hysteresis 0		12	20	45	mV	
V_{HYST1}	Analog comparator hysteresis 1		24	40	85	mV	
V_{HYST2}	Analog comparator hysteresis 2		36	60	130	mV	
DAC_{DNL}	Differential nonlinear		–	±1	–	LSB	

1. ACMP connects to VDD.

6.4.8 SPI Characteristics[1]

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
	f_{func}[2]	Functional frequency	Slave	–	24	MHz
			Master	–	24	MHz
			Master Loopback[4]	–	24	MHz
1	f_{op}	Frequency of operation	Slave	–	12	MHz
			Master	–	12	MHz
			Master Loopback[4]	–	12	MHz
2	t_{SCK}	SCK period	Slave	83.3	–	ns
			Master	83.3	–	ns
			Master Loopback[4]	83.3	–	ns
3	t_{PCSSCK}[5]	PCS to SCK delay	Slave	–	–	ns
			Master	(PCSSCK+1) * t_{delay}[3] - 22	–	ns
			Master Loopback[4]	(PCSSCK+1) * t_{delay}[3] - 22	–	ns
4	t_{SCKPCS}[6]	After SCK delay	Slave	–	–	ns

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Table 27 continued from previous page

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
			Master	(SCKPCS+1) * t_{delay}[3] - 22	–	ns
			Master Loopback[4]	(SCKPCS+1) * t_{delay}[3] - 22	–	ns
5	t_{WSCK}[7]	Clock (SCK) high or low time	Slave	t_{SCK}/2 - 1	t_{SCK}/2 + 1	ns
			Master	t_{SCK}/2 - 1	t_{SCK}/2 + 1	ns
			Master Loopback[4]	t_{SCK}/2 - 1	t_{SCK}/2 + 1	ns
6	t_{setup}	Data setup time (inputs)	Slave	7	–	ns
			Master	27	–	ns
			Master Loopback[4]	5	–	ns
7	t_{holdin}	Data hold time (inputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback[4]	2	–	ns
8	t_{valid}	Data valid (after SCK edge)	Slave	–	33	ns
			Master	–	9	ns
			Master Loopback[4]	–	9	ns
9	$t_{holdout}$	Data hold time (outputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback[4]	0	–	ns
10	$t_{RI/FI}$	Rise/Fall time input	Slave	–	2	ns
			Master	–	2	ns
			Master Loopback[4]	–	2	ns
11	$t_{RO/FO}$	Rise/Fall time output	Slave	–	5	ns
			Master	–	5	ns
			Master Loopback[4]	–	5	ns

1. The trace length for the SCK pad should be kept as short as possible when used in Master loopback mode, and it does not support off-board communication.
2. f_{func} = SPI functional clock, which is generated from IPC.
3. $t_{delay} = (1/f_{op}) * 2^{TXCFG[PRESCALE]}$.
4. Master Loopback mode - In this mode SCK clock is delayed for sampling the input data which is enabled by setting SPI_CTRL[SPDEN] bit as 1.
5. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where PCSSCK ranges from 0 to 255.
6. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where SCKPCS ranges from 0 to 255.
7. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.

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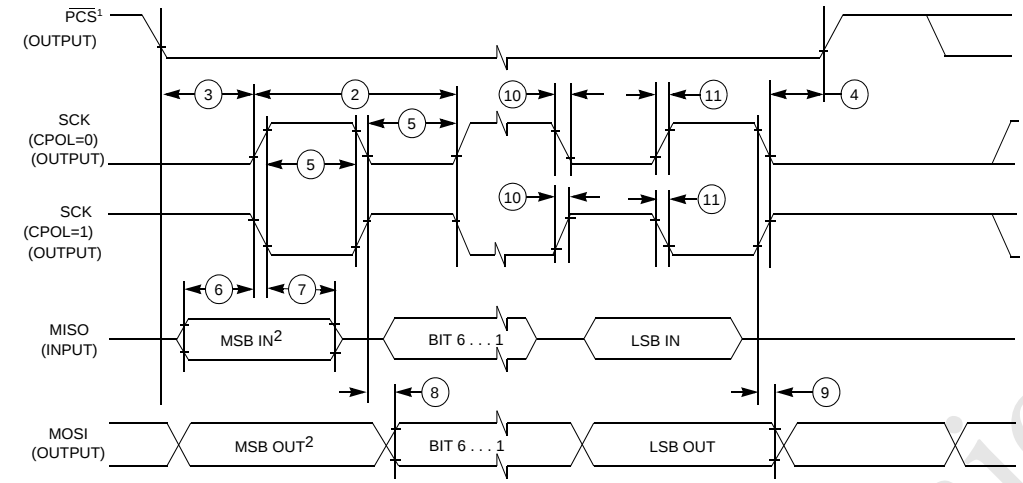
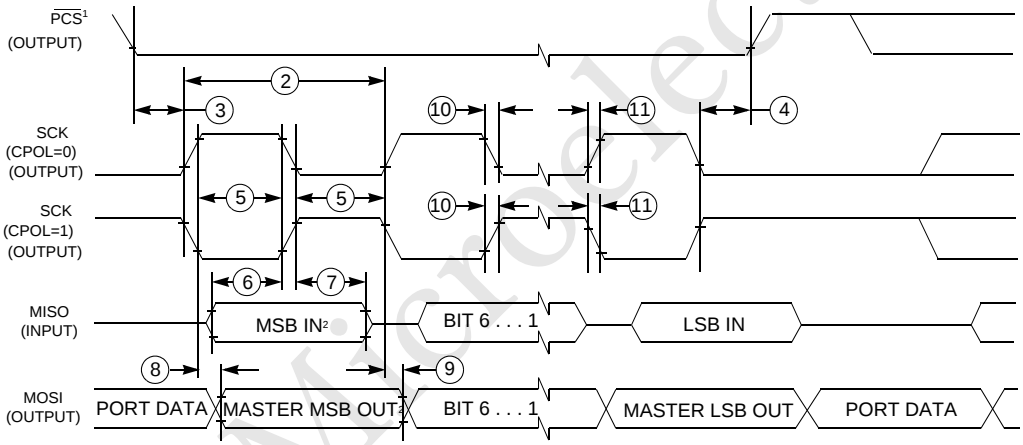


1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11: SPI Master Mode Timing (CHPA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12: SPI Master Mode Timing (CHPA=1)

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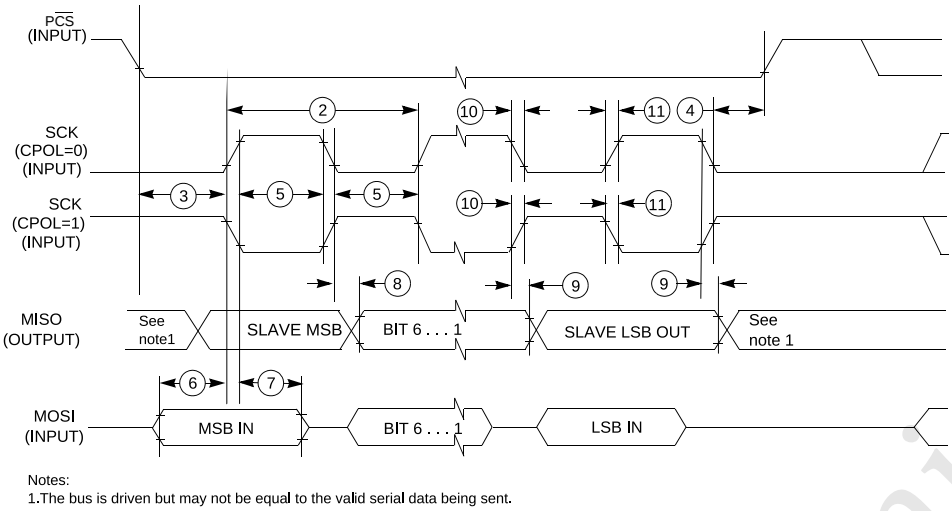

Figure 13: SPI Slave Mode Timing (CHPA=0)

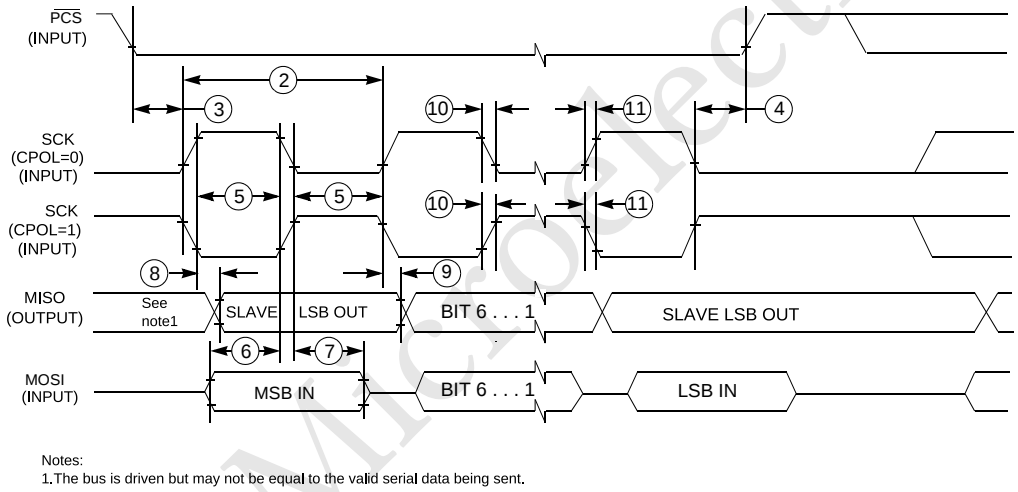

Figure 14: SPI Slave Mode Timing (CHPA=1)

6.4.9 NVM Specifications

6.4.9.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	46	50	53.5	μs	
T_{erase}	Erase execution time	4.0	4.5	5.0	ms	
T_{chip_erase}	Chip erase execution time	30	35	40	ms	

6.4.9.2 Reliability Specifications

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Symbol	Description	Min.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention	20	–	years	
$t_{nvmcycp}$	Cycling endurance	100,000	–	cycles	

6.4.10 Debug Module Electrical

6.4.10.1 SWD Electrical Specifications

Table 30: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

6.4.10.2 SWD Input Clock Timing

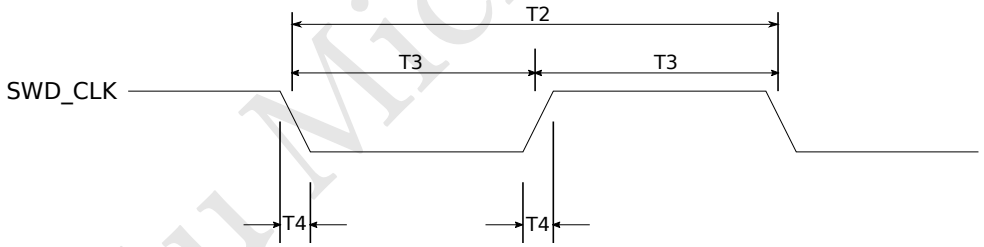

Figure 15: SWD Clock Timing

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6.4.10.3 SWD Output Data Timing

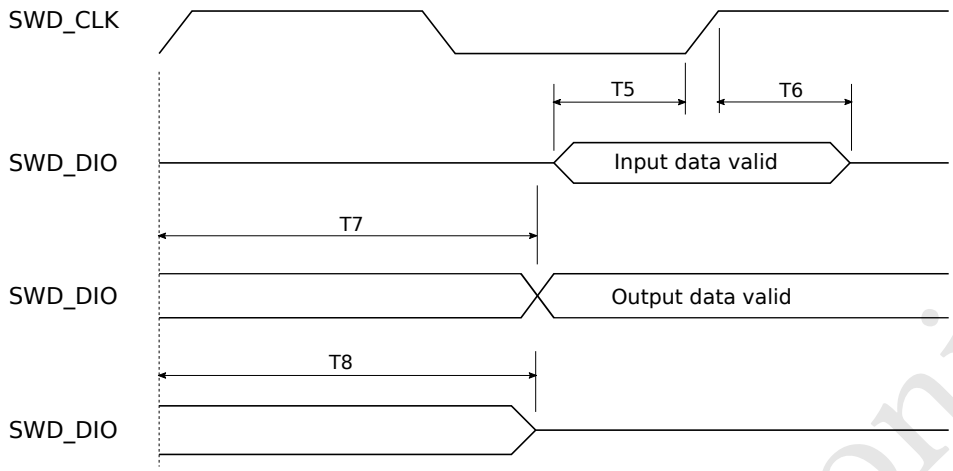

Figure 16: SWD Data Timing

6.5 Thermal Attributes

Table 31: Thermal Characteristics

Package Family	Package Type	Thermal Resistance			Unit
		R_{JA}	R_{JC}	R_{JB}	
LQFP	LQFP32L	89	18	35	°C/W
	LQFP48L	78	16	32	°C/W
	LQFP64L	65	13	30	°C/W
QFN	QFN32L	41	14	16	°C/W

NOTE: Based on environmental simulation per JEDEC standards, the PCB is a JEDEC-compliant 2S2P board. Data in this table is for reference only.

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7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 32: Pinmux Table

64 LQFP	48 LQFP	32 LQFP	32 QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	-	PTD_1	-	PTD_1	eTMR0_CH3	SPI1_SIN	-	I2C1_SCL	-	TMU_OUT2
2	2	2	-	PTD_0	-	PTD_0	eTMR0_CH2	SPI1_SCK	-	I2C1_SDA	-	TMU_OUT1
3	-	-	-	PTE_11	-	PTE_11	SPI2_PCS0	lpTMR0_ALT1	-	-	-	TMU_OUT5
4	-	-	-	PTE_10	-	PTE_10	CLKOUT	SPI2_PCS1	-	-	-	TMU_OUT4
5	3	-	1	PTE_5	-	PTE_5	TCLK_IN2	-	eTMR1_CH1	CAN0_TX	-	-
6	4	-	2	PTE_4	-	PTE_4	CLKOUT	-	eTMR1_CH0	CAN0_RX	-	-
7	5	3	3	VDD	VDD	-	-	-	-	-	-	-
8	6	4	-	VDDA	VDDA	-	-	-	-	-	-	-
9	-	-	-	VREFH	VREFH	-	-	-	-	-	-	-
-	-	5	-	VREFL	VREFL	-	-	-	-	-	-	-
10	7	6	4	VSS	VSS	-	-	-	-	-	-	-
11	8	7	5	PTB_7	EXTAL	PTB_7	I2C0_SCL	-	UART2_TX	-	-	TMU_OUT2
12	9	8	6	PTB_6	XTAL	PTB_6	I2C0_SDA	-	UART2_RX	-	-	TMU_OUT1
13	-	-	-	PTE_3	-	PTE_3	eTMR0_FLT0	SPI1_SIN	-	-	TMU_IN6	ACMP0_OUT
14	10	-	7	PTD_16	EXTAL32K	PTD_16	eTMR0_CH1	-	SPI0_SIN	ACMP0_ACTIVE	-	-
15	11	-	8	PTD_15	XTAL32K	PTD_15	eTMR0_CH0	-	SPI0_SCK	-	-	-
16	12	-	-	PTE_9	-	PTE_9	eTMR0_CH7	SPI1_SCK	-	-	-	-
17	13	-	9	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	-	-	-	-	-
18	14	9	10	PTB_5	-	PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	CLKOUT	TMU_IN0	-
19	15	10	11	PTB_4	-	PTB_4	eTMR0_CH4	SPI0_SOUT	-	-	TMU_IN1	-
20	16	11	12	PTC_3	ADC0_SE11 ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	UART0_TX	-	-	-
21	17	12	13	PTC_2	ADC0_SE10 ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	UART0_RX	-	-	-
22	-	-	-	PTD_7	ACMP0_IN6	PTD_7	UART2_TX	eTMR0_CH3	-	-	-	-
23	-	-	-	PTD_6	ACMP0_IN7	PTD_6	UART2_RX	eTMR0_CH2	-	-	-	-
24	18	-	14	PTD_5	-	PTD_5	-	lpTMR0_ALT2	-	-	TMU_IN7	-
25	19	13	-	PTC_1	ADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT	SPI2_SIN	-	eTMR1_CH7	-
26	-	14	-	PTC_0	ADC0_SE8	PTC_0	eTMR0_CH0	SPI2_SIN	SPI2_PCS1	-	eTMR1_CH6	-
27	-	-	-	PTC_17	ADC0_SE15	PTC_17	eTMR1_FLT3	-	SPI2_PCS2	-	-	-
28	20	-	-	PTC_16	ADC0_SE14	PTC_16	eTMR1_FLT2	-	SPI2_SCK	-	-	-
29	21	-	-	PTC_15	ADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK	SPI2_SOUT	-	TMU_IN8	-
30	22	-	-	PTC_14	ADC0_SE12	PTC_14	eTMR1_CH2	-	SPI2_PCS0	-	TMU_IN9	-
31	23	15	15	PTB_3	ADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	-	TMU_IN2	-
32	24	16	16	PTB_2	ADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	-	TMU_IN3	-
33	25	17	17	PTB_1	ADC0_SE5	PTB_1	UART0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	-	-
34	26	18	18	PTB_0	ADC0_SE4	PTB_0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	-	-
35	27	-	-	PTC_9	-	PTC_9	UART1_TX	eTMR1_FLT1	-	-	-	-

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64 LQFP	48 LQFP	32 LQFP	32 QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
36	28	-	-	PTC_8	-	PTC_8	UART1_RX	eTMR1_FLT0	-	-	-	-
37	29	19	19	PTA_7	ADC0_SE3	PTA_7	eTMR0_FLT2	-	RTC_CLKIN	-	-	-
38	-	20	-	PTA_6	ADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1	-	-	-	-
39	-	-	-	PTE_7	-	PTE_7	eTMR0_CH7	SPI1_PCS2	-	-	-	-
40	30	-	20	VSS	VSS	-	-	-	-	-	-	-
41	31	-	21	VDD	VDD	-	-	-	-	-	-	-
42	32	-	-	PTB_13	-	PTB_13	eTMR0_CH1	-	-	-	-	-
43	-	-	-	PTB_12	-	PTB_12	eTMR0_CH0	-	-	-	-	-
44	-	-	-	PTD_4	-	PTD_4	eTMR0_FLT3	-	-	-	-	-
45	33	21	22	PTD_3	-	PTD_3	-	SPI1_PCS0	I2C1_SCL	eTMR2_CH0	TMU_IN4	NMI_b
46	34	22	-	PTD_2	-	PTD_2	-	SPI1_SOUT	I2C1_SDA	eTMR2_CH1	TMU_IN5	-
47	35	23	23	PTA_3	-	PTA_3	eTMR2_CH0	I2C0_SCL	SPI2_SCK	-	UART0_TX	-
48	36	24	24	PTA_2	-	PTA_2	eTMR2_CH1	I2C0_SDA	SPI2_SIN	-	UART0_RX	-
49	37	25	25	PTA_1	ADC0_SE1 ACMP0_IN1	PTA_1	eTMR1_CH1	-	SPI2_SOUT	eTMR1_QD_PHA	-	TMU_OUT0
50	38	26	26	PTA_0	ADC0_SE0 ACMP0_IN0	PTA_0	eTMR1_CH0	-	SPI2_PCS0	-	-	TMU_OUT3
51	39	27	-	PTC_7	-	PTC_7	UART1_TX	-	SPI2_PCS1	CAN0_TX	eTMR1_QD_PHA	-
52	40	28	-	PTC_6	-	PTC_6	UART1_RX	-	-	CAN0_RX	eTMR1_QD_PHB	-
53	-	-	-	PTE_6	-	PTE_6	SPI0_PCS2	-	-	-	-	-
54	-	-	-	PTE_2	-	PTE_2	SPI0_SOUT	lpTMR0_ALT3	-	-	-	-
55	41	-	-	PTA_13	-	PTA_13	eTMR1_CH7	-	-	UART2_TX	-	-
56	42	-	-	PTA_12	-	PTA_12	eTMR1_CH6	-	-	UART2_RX	-	-
57	43	-	27	PTA_11	-	PTA_11	eTMR1_CH5	-	I2C1_SCL	ACMP0_ACTIVE	-	-
58	44	-	28	PTA_10	-	PTA_10	eTMR1_CH4	-	I2C1_SDA	-	-	-
59	-	-	-	PTE_1	-	PTE_1	SPI0_SIN	-	I2C1_SCL	SPI1_PCS0	eTMR1_FLT1	-
60	-	-	-	PTE_0	-	PTE_0	SPI0_SCK	TCLK_IN1	I2C1_SDA	SPI1_SOUT	eTMR1_FLT2	-
61	45	29	29	PTC_5	-	PTC_5	eTMR2_CH0	RTC_CLKOUT	eTMR1_CH1	-	-	-
62	46	30	30	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT	-	-	eTMR1_QD_PHB	SWD_CLK
63	47	31	31	PTA_5	-	PTA_5	-	TCLK_IN1	-	-	-	RESET_b
64	48	32	32	PTA_4	-	PTA_4	-	-	ACMP0_OUT	-	-	SWD_IO

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7.2 Packages

The information of package pinouts is as follows:

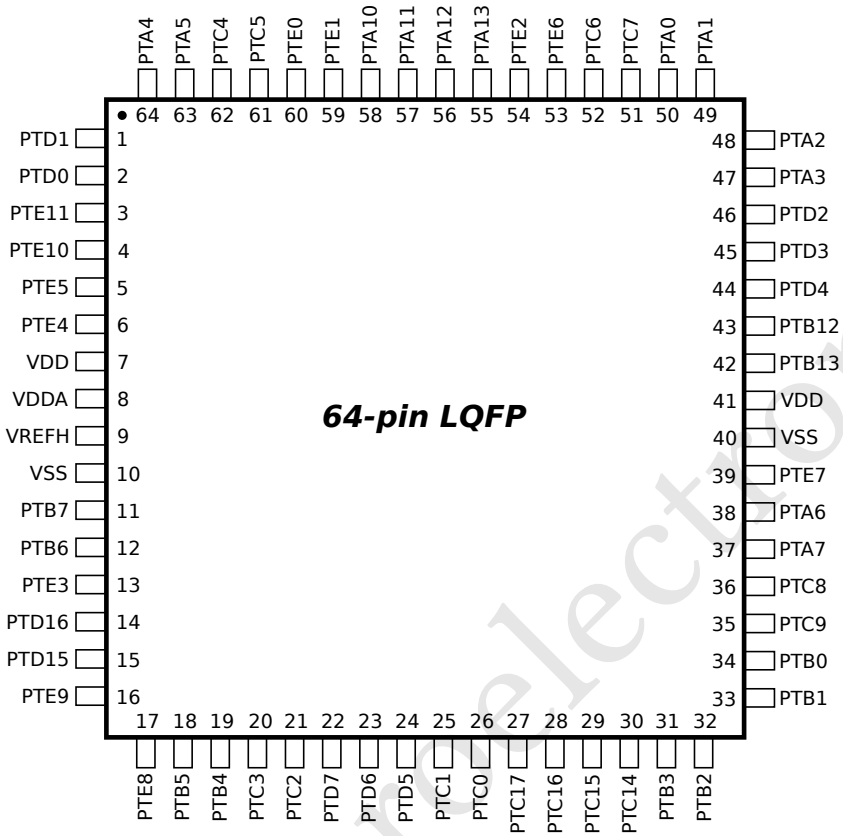

Figure 17: 64-pin LQFP Package

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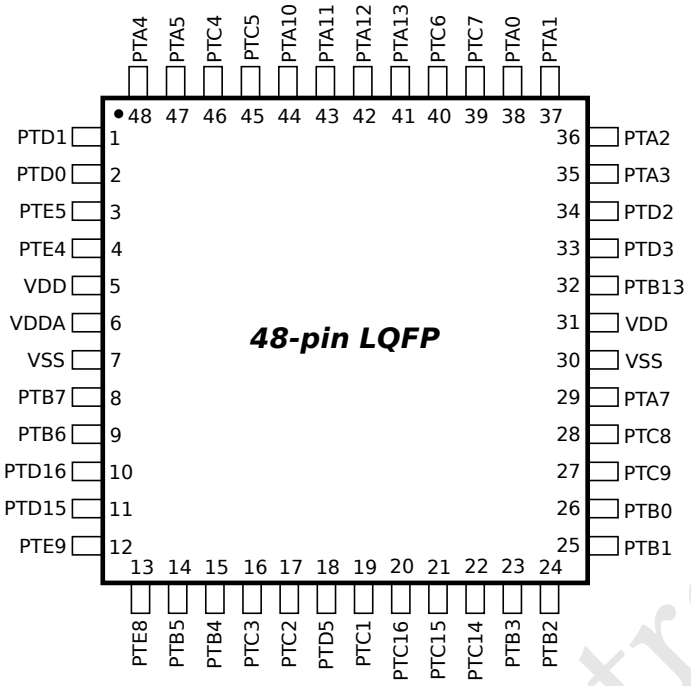

Figure 18: 48-pin LQFP Package

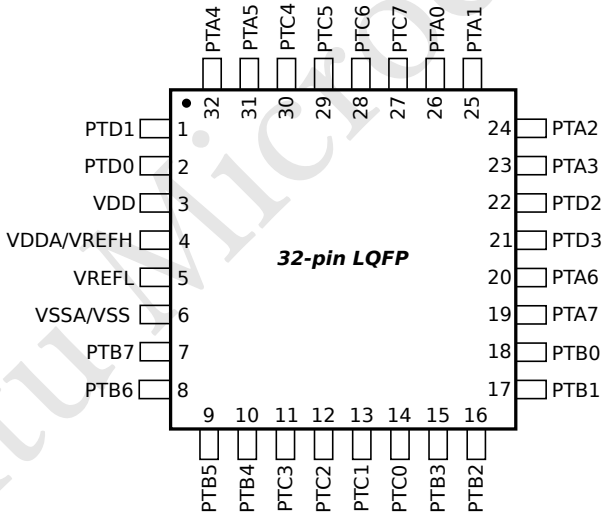

Figure 19: 32-pin LQFP Package

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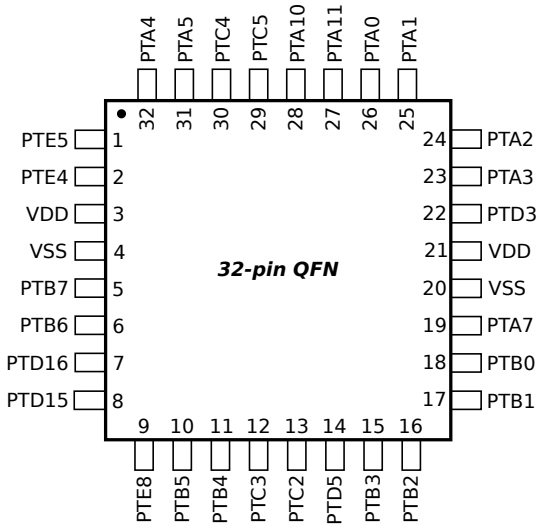

Figure 20: 32-pin QFN Package

Note: The chip mark will not contain packing information(T/R)

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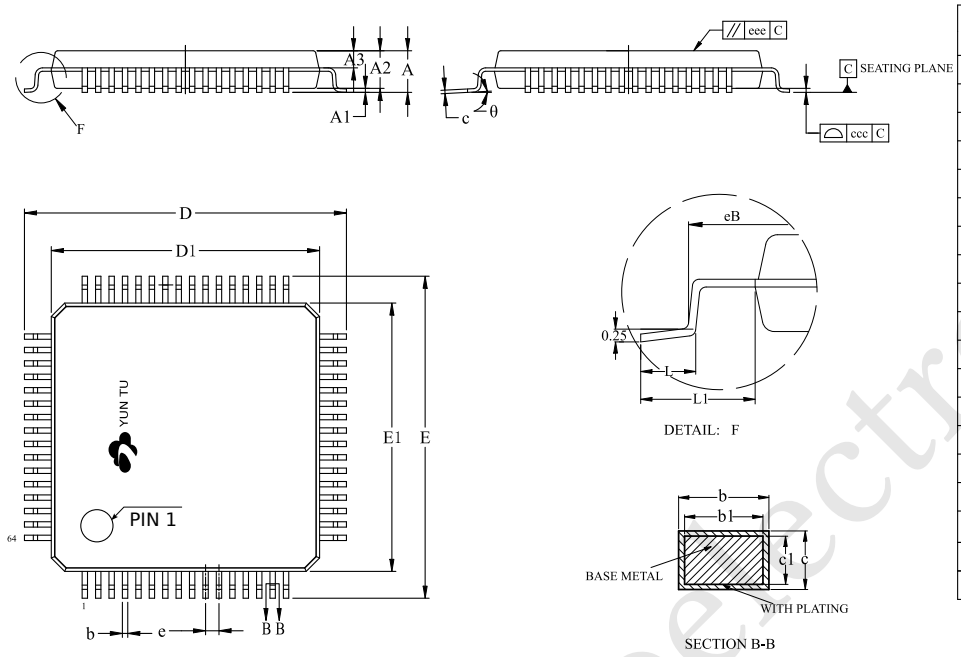
7.3 Dimensions

Package dimensions are as follows:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°
eee	0.10		
ccc	0.08		

Figure 21: 64pin LQFP

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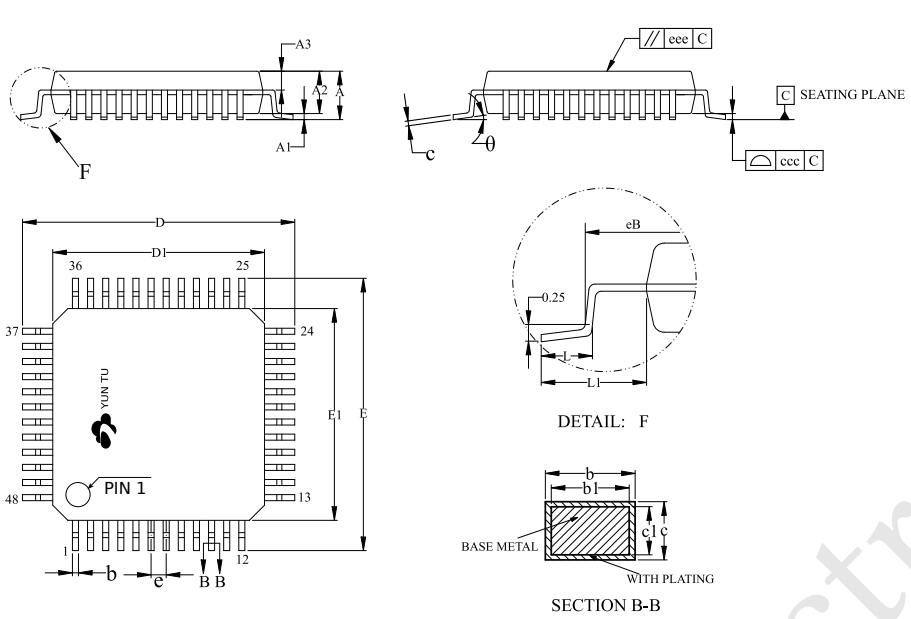

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°
eee	0.10		
ccc	0.08		

Figure 22: 48pin LQFP

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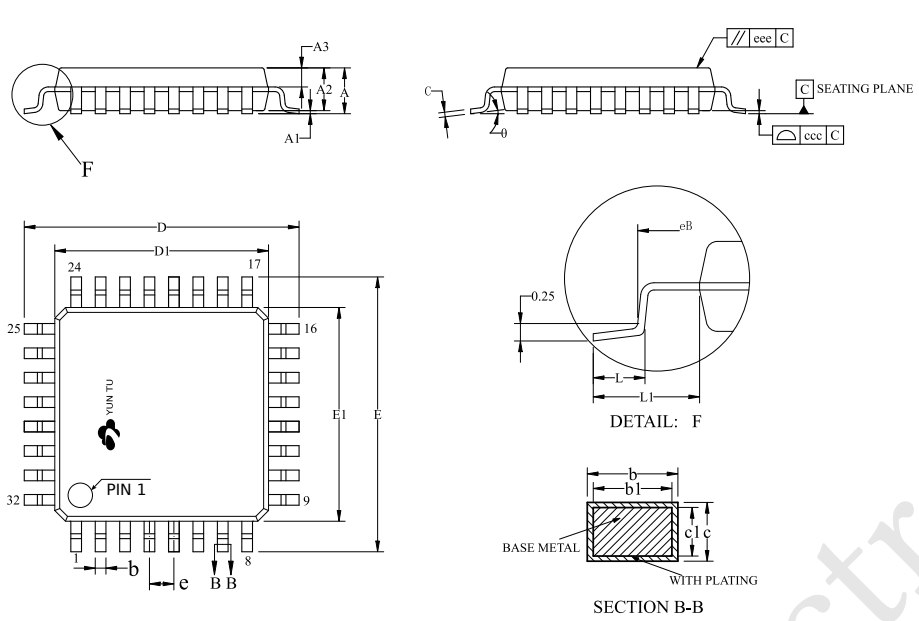

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°
eee	0.10		
ccc	0.10		

Figure 23: 32pin LQFP

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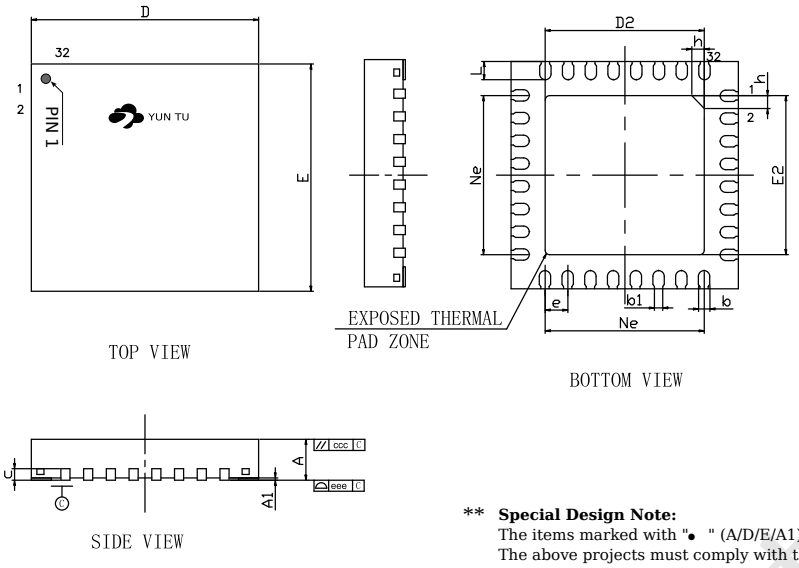

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
● A	0.80	0.85	0.90
● A1	—	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
e	0.18	0.20	0.25
● D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
● E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
ccc	0.10		
eee	0.08		

** **Special Design Note:**
The items marked with "● " (A/D/E/A1) are key characteristics.
The above projects must comply with the management and control requirements of automotive electronic projects.

Figure 24: 32pin QFN

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7.4 Reflow Profile Guideline

Reflow Condition:

- ➢ can guarantee 3X IR reflow base on the Reflow profile(Figure 5-1) guideline in IPC/JEDEC J-STD-020E;
- ➢ Preheat/Soak: Pb-Free Assembly for 150°C~200°C for 60~120s;
- ➢ Average ramp-up rate(Ts to peak):3°C/second max.;
- ➢ Liquidous temperature maintained above Pb-Free 217°C for 60-150s;
- ➢ Time (tp)* within 5°C of the specified classification temperature Pb-Free 30s ;
- ➢ Note :

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in this table.
For example, if Tc is 260°C and time Tp is 30 seconds, this means the following for the supplier and the user:
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Table 4-2 Pb-Free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Table 5-2 Classification Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.		

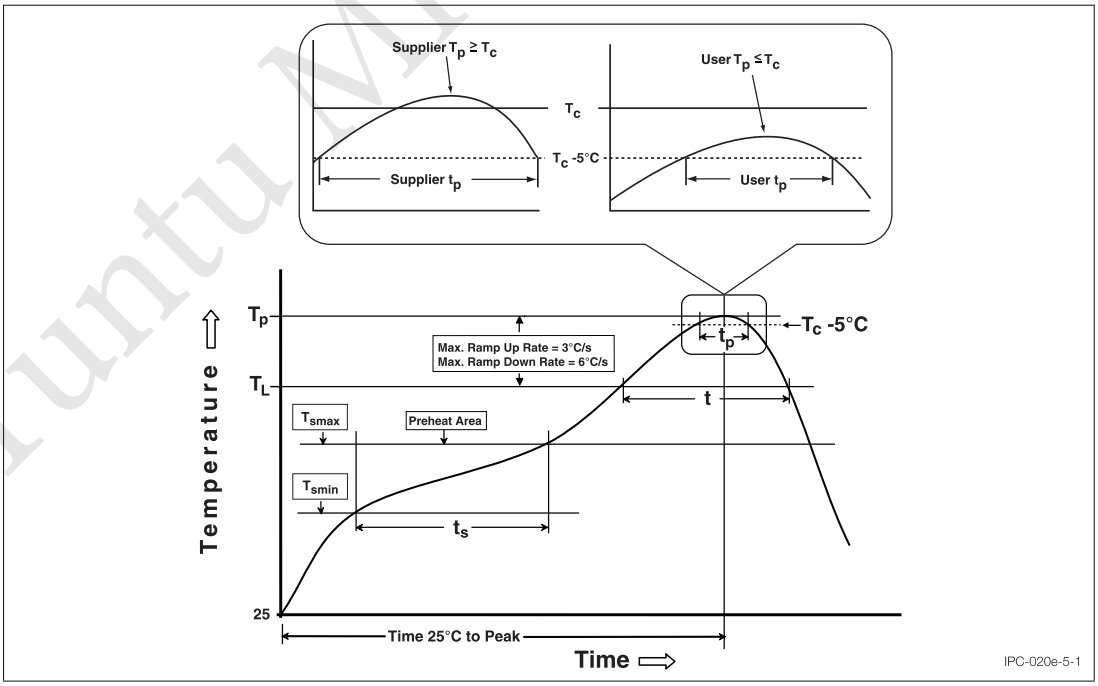

Figure 5-1 Classification Profile (Not to scale)

Figure 25: Reflow Profile Guideline

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Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2022/10/17	Initial version
1.1	2022/12/19	Changed maximum value from 150 to 135 in the second row of 'Thermal Operating Characteristics' table. Changed V_{LAT} to I_{LAT} in 'ESD Handling Ratings' table. Updated FIRC frequency accuracy information and changed the min value to -1.5, max value to 1.5 in 'FIRC(48MHz) Characteristics' table.
1.2	2023/4/28	Added the whole chapter of 'Features' Updated the value of V_{HBM} in 'ESD Handling Ratings' Added the note of 5.8 in 'Absolute Maximum Ratings' Updated the contents of 'Voltage and Current Operating Requirements' Updated the value of I_{leak} and I_{IN} of 'DC Electrical Specifications at 3.3V' Updated the value of I_{leak} and I_{IN} of 'DC Electrical Specifications at 5.0V' Updated the typical value in 'Power Consumption' Corrected the value of Max to Typ in 'Device Clock Specifications' Updated the contents of 'FXOSC(4-40MHz) Characteristics' Updated the contents of 'SXOSC(32.768KHz) Characteristics' Updated the contents of 'ACMP Characteristics' Added the new section of 'Thermal Attributes' Updated the table in the figure of 32pin QFN
1.3	2023/5/23	Updated the table of 'Ordering Information' Added the pinmux table of YTM32B1LE04x in 'IO Signal Description'
1.4	2023/6/15	Added the coplanarity specifications of product in the section of 'Dimensions' Added the location information of PIN 1 in the section of 'Dimensions'
1.5	2023/7/21	Updated the content in the table of 'Ordering Information' Added the new section of 'Power Up Requirements' Updated the content in the section of 'IO Signal Description'
1.6	2023/8/14	Updated the ordering information and part numbers in 'Ordering information' Updated the figure and table in 'Power and Ground Pins' Updated the power up time in 'Power Up Requirements' Updated the figure and first table in 'ADC Characteristics'
1.7	2023/10/8	In section Ordering Information, table 'Ordering Information', removed cost versions. In subsection Power Consumption, updated the description of 'SIRC' core and 'FXOSC' core.
1.8	2024/9/20	Added the information about ASIL-B in the chapter of 'Features' Updated all package dimensions in the section of 'Dimensions'
1.9	2024/12/5	Updated supply voltage 2.7V to 2.97V in the whole Data Sheet Added Min and Max value in subsection of 'Moisture Handling Ratings' Added Min and Max value in subsection of 'ESD Handling Ratings' Added Min and Max value in subsection of 'Absolute Maximum Ratings' Added Min and Max value in subsection of 'Voltage and Current Operating Requirements' Added Min and Max value in subsection of 'DC Electrical Specifications at 3.3V' Added Min and Max value in subsection of 'DC Electrical Specifications at 5.0V' Added Min and Max value in subsection of 'Power and Ground Pins' Added Min and Max value in subsection of 'POR,LVR and LVD Operating Requirements' Added Min and Max value in subsection of 'Power Consumption' Added the whole subsection of 'Power Supply Fluctuation Requirements' Added Min and Max value in subsection of 'FXOSC(4-40MHz) Characteristics' Added Min and Max value in subsection of 'FIRC(48MHz) Characteristics' Added Min and Max value in subsection of 'SXOSC(32.768KHz) Characteristics' Added Min and Max value in subsection of 'SIRC(2MHz) Characteristics' Added Min and Max value in subsection of 'LPO(750Hz) Characteristics' Added Min and Max value in subsection of 'ADC Characteristics' Added Min and Max value in subsection of 'ACMP Characteristics'
2.0	2025/2/27	Updated Max value of V_{VDDA} and V_{REFH} in subsection of 'Voltage and Current Operating Requirements' Updated the description in subsection of 'Power Supply Fluctuation Requirements' Updated format of table about gain selection in subsection of 'FXOSC(4-40MHz) Characteristics' Removed the subsubsection of 'Flash High Voltage Current Behaviors'
2.1	2025/9/1	Added the value of T_{ramp} in subsection of 'Voltage and Current Operating Requirements' Added the whole subsubsection of 'MCU Power Supply Ramp Rate' Corrected Min value of V_{IN} in subsection of 'ACMP Characteristics' Added the whole subsection of 'SPI Characteristics' Added the value of R_{JC}, R_{JB} and note in the section of 'Thermal Attributes' Corrected the name of PIN9 to "PTE8" of QFN32 package in section of 'Packages'

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Rev.No.	Date	Substantive Change(s)
2.2	2026/1/8	Added the chip storage conditions in subsection of 'Moisture Handling Ratings' Updated the symbol and value in subsection of 'POR,LVR and LVD Operating Requirements' Updated the information of gm in subsection of 'FXOSC(4-40MHz) Characteristics' Added the clock source information in subsection of 'FIRC(48MHz) Characteristics' Updated the information of gm in subsection of 'SXOSC(32.768KHz) Characteristics' Added the clock source information in subsection of 'SIRC(2MHz) Characteristics' Added the section of "Reflow Profile Guideline" in chapter of 'Pinouts'

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