Errata Sheet

YTM32B1LE0

This document details the silicon errata known at the time of publication for the YTM32B1LE0 device. For additional information, please see YTM32B1LE0 Reference Manual or Data sheet.

Revision History

Rev.No.	Date	Substantive Change(s)
1.7	2025-12-25	Added PCU errata E110003
1.6	2025-09-03	Added PCU errata E110002 Updated workaround for SPI errata E403002 Added ADC errata E600007 Removed CMU errata E715002
1.5	2025-04-29	Added E110001 PCU errata
1.4	2025-04-07	E0003 eTMR errata ID is updated to E503001 E0006 DMA errata ID is updated to E010003 E0007 I2C errata ID is updated to E407001 E0008 GPIO errata ID is updated to E300001 E0009 GPIO errata ID is updated to E300002 E0010 DMA errata ID is updated to E010001.A E0012 eTMR errata ID is updated to E503003 Removed E0013 eTMR errata E0019 eTMR errata ID is updated to E503005 E0021 CLOCK errata ID is updated to E130001 Added E010002 DMA errata Added E300003, E300004 GPIO errata Added E403001, E403002, E403003 SPI errata Added E405001 UART errata Added E502001 LPTMR errata Added E503009 eTMR errata Added E509001 RTC errata Added E600004, E600005 ADC errata Added E706001 CRC errata Added E715002 CMU errata
1.3	2024-10-28	Updated E0010 DMA, remove LINFlexD relative description Added E0019 eTMR Added E0021 CLOCK
1.2	2024-08-16	Added E0009 GPIO Added E0010 DMA Added E0012 eTMR Added E0013 eTMR
1.1	2024-02-27	Added E0006 DMA Added E0007 I2C Added E0008 GPIO
1.0	2023-12-02	Initial version

Table 2: Errata Table

Erratum ID	Erratum Title
E010001.A	[DMA] DMA may respond to the module request one more time
E010002	[DMA] DMA REQEN register modify write may interfere with other channel(s)
E010003	[DMA] DMA will halt CPU if fast bus clock is lower than core clock
E110001	[PCU] Low-probability power-up failure at reduced VDD voltage
E110002	[PCU] BORLPMD functional issue under unstable VDD condition
E110003.A	[PCU] VDD15 LVD Lacks Interrupt/Reset Support; Requires Polling Implementation
E130001	[IPC] Very low probability of IPC functional clock divider not working
E300001	[GPIO] An unexpected interrupt will be generated when using filter after GPIO is configured as low-level or falling edge triggering
E300002	[GPIO] Write GPIO registers may clear interrupt flags
E300003	[GPIO] When SXOSC is selected as GPIO filter clock, there may be an unexpected interrupt after GPIO falling edge wake-up
E300004	[GPIO] Slow transition edges (both rising/falling) on GPIO inputs can induce spurious interrupts
E403001	[SPI] RXFIFO overflow flag logic error
E403002	[SPI] TXCFG register read value keep old after writing
E403003	[SPI] In SPI master mode, enabling both PCS continuous mode and TX mask simultaneously will result in continuous clock output
E405001	[UART] Clear match flag bit mismatch
E407001	[I2C] In I2C slave mode, turning on tx stall may cause I2C master arbitration to fail
E502001	[LPTMR] When polling to read CCF, there is a small probability of reading incorrect flag information
E503001	[eTMR] 100% duty cycle can not be generated through configuring VAL0 and VAL1 register
E503003	[eTMR] The channel 2-7 DMA requests of eTMR1 and eTMR2 will not be cleared by DMA done
E503005	[eTMR] The channel flag will be set if channel capture event occurs before counter enable
E503009	[eTMR] Write 0 to LDOK bit will clear this bit
E509001	[RTC] Alarm/Seconds/Overflow flag will not be set again after write 1 clear
E600004	[ADC] A reduction in VDD voltage to 2.7V may lead to a performance degradation in ADC
E600005	[ADC] When the ADC bus clock frequency differs greatly from the function clock frequency, the problem of multiple interrupts may occur
E600007	[ADC] TMU Trigger Source ADC0_COCO for Monitoring ADC Conversion Status
E706001	[CRC] Writing high 16 bits data to DATA register is invalid

E010001.A: [DMA] DMA may respond to the module request one more time

Description 描述

When the DMA trigger count is greater than 1, if a low-speed peripheral triggers a DMA request, the DMA may respond to a peripheral request as two requests. Affected peripherals include lpTMR, ACMP, SPI_END_OF_PACKET and UART_IDLE requests. However, SPI and UART module RX and TX DMA requests are not affected.

当 DMA 触发计数大于 1 时，如果使用低速外设触发 DMA 请求，DMA 可能会将一次外设请求响应为两次。受影响的外设包括 lpTMR、ACMP、SPI_END_OF_PACKET 和 UART_IDLE 请求。而 SPI 和 UART 模块的 RX 和 TX 的 DMA 请求不受影响。

Workaround 规避方案

Use the DMA request of eTMR instead of lpTMR, while other modules should avoid using DMA requests and instead use interrupt handling.

对于 lpTMR 模块可以使用 eTMR 的 DMA 请求来替代，而其他模块应避免使用 DMA 请求，而是采用中断方式进行处理。

E010002: [DMA] DMA REQEN register modify write may interfere with other channel(s)

Description 描述

When user adds new channel request, in order not to lose original channel request, normally first read REQEN[CH], and then OR with the new channel, finally write to REQEN register. However, one case is that the original channel transfer has completed in the period of reading and writing REQEN regisetr, thus, the original channel request will be enabled again, an unexpected transfer will be triggered.

当用户添加新的通道传输请求时，为了不丢失原有通道的传输请求，一般会先读取 REQEN[CH]，再或上新加的通道，再写入 REQEN[CH]。然而有一种情况是在读取之后，写入之前的这段时间原有通道的传输正好完成，这样就又会使能原有通道的传输请求，那么就会触发意外的 DMA 传输。

Workaround 规避方案

User needs to pause the original channel transfer before operating REQEN register, at this time, it is necessary to wait until the channel active is low (i.e., no dma channel is busy), and then execute the BSET operation on the REQEN register. After the operation is completed, clears PAUSE.

用户在对 REQEN 寄存器位操作前需置位 CTRL[PAUSE] 来暂停原有通道的传输，此时需要等到通道 active 为低（即没有 DMA 通道忙），然后再进行对 REQEN 寄存器进行位操作。操作完成之后清除 CTRL[PAUSE]。

E010003: [DMA] DMA will halt CPU if fast bus clock is lower than core clock

Description 描述

When the fast bus clock and core clock frequencies are different, DMA register access will cause the core to stop running.

当快速总线时钟和内核时钟不同频时，DMA 的寄存器访问会造成内核停止运行。

Workaround 规避方案

Keep the default core clock and fast bus clock frequency ratio of 1:1, or avoid using DMA in applications where fast bus clock needs to be configured lower than core clock.

保持默认的内核时钟和快速总线时钟频率比为 1:1，或者在需要配置快速总线时钟为低于内核时钟的应用中避免使用 DMA。

E110001: [PCU] Low-probability power-up failure at reduced VDD voltage

Description 描述

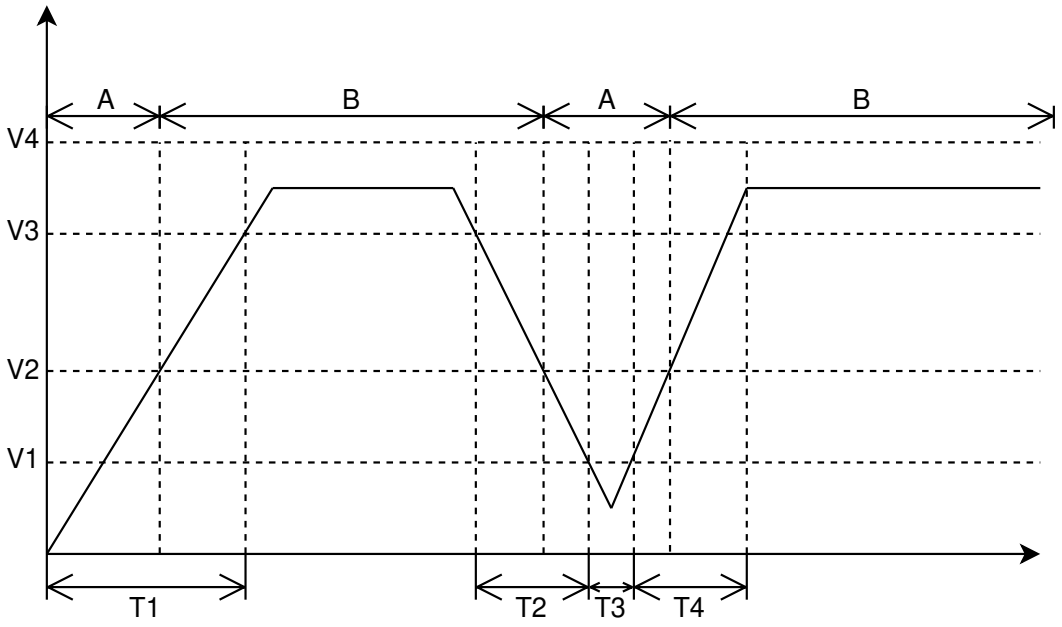
When the VDD supply voltage falls within the range of 400–600 mV during power-down, there is a low but non-zero probability that the chip may fail to power up correctly on subsequent reinitialization.

当电源电压 VDD 在断电过程中下降至 400-600 mV 区间时，芯片存在极低概率无法正常上电的情况。

Power-up/down timing 断电/上电时序

It is necessary to ensure that the VDD supply voltage meets the following timing requirements during power-up or power-down:

在电源上电或断电过程中，VDD 供电电压必须满足以下时序要求：



A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 1: Power timing requirements

Symbol	Name	Description	Unit(V)
V_1	Restart threshold voltage[重新上电阈值电压]	When power up MCU again, VDD should keep below V_1 for a period of T_3.[当 MCU 重新上电时，VDD 应保持低于 V_1 一段时间 T_3 再上升。]	0.2
V_2	Minimum MCU operating voltage[MCU 最小工作电压]	The MCU starts working when VDD reaches V_2.[当 VDD 达到 V_2 时，MCU 开始工作。]	2.5
V_3	Lower voltage limit of MCU operating normally[MCU 正常工作电压下限]	Minimum operating voltage for normal MCU operation and interaction with peripherals.[MCU 正常工作以及内核与外设交互的最小工作电压。]	2.97
V_4	Upper voltage limit of MCU operating normally[MCU 正常工作电压上限]	Maximum operating voltage for normal MCU operation and interaction with peripherals.[MCU 正常工作以及内核与外设交互的最大工作电压。]	5.5

Symbol	Name	Description	Unit(s)
T_1	Power-up time[上电时间]	Rising time of MCU VDD from 0 to V_3.[MCU VDD 从 0V 上升到 V_3 的时间。]	10 μs < T_1 < 50 ms
T_2	Power-down time[掉电时间]	Falling time of MCU VDD from V_3 to V_1 during the MCU power up/down process.[在 MCU 上下电过程中，VDD 从 V_3 下降到 V_1 的时间。]	10 μs < T_2 < 500 ms

Symbol	Name	Description	Unit(s)
T_3	Restart threshold voltage retain time[重新上电阈值电压保持时间]	Minimum duration of MCU VDD below V_1 when powering up again.[MCU 重新上电时 VDD 在低于 V_1 的最小持续时间。]	T_3 > 100 μs
T_4	Restart power-up time[重新上电时间]	Time required for MCU VDD to rise from V_1 to V_3.[MCU 重新上电时 VDD 从 V_1 上升到 V_3 的时间。]	10 μs < T_4 < 50 ms

NOTE:

1. The power-up process needs to be restarted if a VDD voltage drop occurs during the T_1/T_4 power-up process before the VDD voltage reaches the V_2 voltage.
2. Restarting the power-up of MCU needs to ensure that the voltage of VDD continues to drop below V_1 and remains there for T_3 time.

注意:

1. 如果在 T_1 或 T_4 时间段的上电过程中，在 VDD 电压达到 V_2 前掉落，则需要重新启动电源上电过程。
2. 掉电后重新上电时需要确保 VDD 持续下降至 V_1 以下，并保持在 V_1 以下状态一段时间 T_3。

Workaround 规避方案

For applications with low power consumption, it is recommended to use a small capacitor (1-10 μF) on the VDD pin to avoid excessively long discharge time.

对于有低功耗需求的应用，VDD 上的电容容值不宜过大，避免放电时间过长，建议使用 1-10 μF。

For applications with power-down, to ensure reliable power cycling, connect a bleed resistor (recommended value: 1 KΩ, depending on system impedance) between the VDD pin and ground. This resistor accelerates VDD discharge, guaranteeing that the supply voltage decays below 200 mV (the safe reset threshold) within the required timeframe.

对于有断电需求的应用，在 VDD 引脚与地之间串联泄放电阻（推荐阻值：1 KΩ，具体值需根据系统阻抗确定），以确保断电时 VDD 电压能快速放电至 200 mV（安全复位阈值）以下。

E110002: [PCU] BORLPMD functional issue under unstable VDD condition

Description 描述

When the BORLPMD (Brown-Out Reset Low-Power Mode) feature is enabled, the BOR function is periodically switched on and off. If a rapid fluctuation in the VDD supply voltage occurs during the interval when BOR circuit is disabled, the system fails to generate a BOR reset signal. As a result, the chip is not properly reset, leading to unexpected system behavior or operational faults.

当使能 BORLPMD（低功耗模式欠压复位）功能时，BOR 电路会周期性开关。若在 BOR 电路处于关闭状态时，VDD 电源出现瞬态波动，系统将无法产生 BOR 复位信号。因此，芯片可能无法正常复位，从而导致意外运行或故障。

Workaround 规避方案

In applications where the VDD supply is prone to instability, it is recommended to avoid disabling the BOR function. The BORLPMD mode should not be enabled. Instead, BOREN and BORLPMD bits must not be modified to keep the following configuration:

Set BOREN = 1 (BOR enabled) Set BORLPMD = 0 (BOR low-power mode disabled)

This ensures that the BOR circuit remains active continuously and can respond appropriately to voltage variations.

在 VDD 电源易出现不稳定的应用中，强烈建议保持 BOR 功能开启，并禁用 BORLPMD 模式。必须保持如下配置，请勿修改相应寄存器位：

设置 BOREN = 1（使能 BOR 功能）设置 BORLPMD = 0（禁用 BOR 低功耗模式）

该配置可确保 BOR 电路持续工作，从而能够正确响应电压变化。

E110003.A: [PCU] VDD15 LVD Lacks Interrupt/Reset Support; Requires Polling Implementation

Description 描述

The VDD15 Low-Voltage Detect (LVD) circuit lacks hardware support for generating interrupt requests or system reset signals. Error detection is dependent solely on software polling of status register flags. Additionally, the electrical characteristics of the internal VDD15 LVD module may exhibit unit-to-unit variation. Consequently, operational accuracy and reliability across full operating conditions are not explicitly guaranteed.

VDD15 低电压检测 (LVD) 电路缺乏生成中断请求或系统复位信号的硬件支持。错误检测完全依赖于对状态寄存器的软件轮询操作。此外，内部 VDD15 LVD 模块的电气特性可能存在个体差异性。因此，其在全工作条件下的运行准确性和可靠性不作明确保证。

Workaround 规避方案

It is recommended to implement the on-chip ADC peripheral to perform periodic sampling of the VDD15 power rail. When integrated with a high-priority software routine executing at appropriate intervals, this method provides a deterministic and verifiable approach to achieve required error detection latency requirements. Implementation details are provided in related application note.

建议利用片内 ADC 外设实现对 VDD15 电源的周期性采样。当与适当间隔执行的高优先级软件例程结合使用时，该方法可提供一种确定性且可验证的方案来满足错误检测的延迟要求。具体实现细节请参考相关应用笔记。

E130001: [IPC] Very low probability of IPC functional clock divider not working

Descriptions 描述

When the IPC functional clock and system clock operate in different clock domains and the functional clock frequency is lower than the system clock(both functional clock and system clock are working properly), there is an extremely low probability that the functional clock divider will not work properly when the functional clock divider value is repeatedly switched. In such cases, the functional clock will maintain its previous divider value.

当 IPC 选择的功能时钟和系统时钟不同源且频率低于系统时钟时（功能时钟和系统时钟都正常工作），反复切换功能时钟分频系数时有极低概率会出现 IPC 分频器无法正常工作的状况。分频器不工作情况下功能时钟会维持之前的分频值。

Workaround 规避方案

The using method are as follows:

1. Avoid updating the functional clock divider during the running process.
2. When using SXOSC or FXOSC as functional clock source, firstly disable the clock source, then update functional clock divider value, finally enable the corresponding clock source.
3. When the selected IPC functional clock is not synchronized with the system clock, the divider value should maintain the default value 1 (register value is 0). If they are synchronized, other division factors can be configured (non-zero register value).

使用方法如下：

1. 避免在运行过程中更新功能时钟分频值。
2. 当使用 SXOSC 或 FXOSC 作为功能时钟源时，应该先关闭对应时钟源，然后更新功能时钟分频值，最后再开启对应时钟源。
3. 如果选择的 IPC 功能时钟与系统时钟不同源时，分频值应当保持默认 1 分频（寄存器值为 0）。如果同源，那么分频值可以配其它分频值（寄存器值非 0）。

E300001: [GPIO] An unexpected interrupt will be generated when using filter after GPIO is configured as low-level or falling edge triggering

Description 描述

When the GPIO module is configured as input mode with the filter, and interrupt trigger condition is low-level or falling edge, an unexpected interrupt will be generated.

当 GPIO 配置成带有过滤器的输入模式，中断触发为低电平或者下降沿触发时，此时会发生意外中断。

Workaround 1 规避方案 1

A possible approach is to first configure the GPIO Filter, then clear the flag, and finally set up the GPIO interrupt. The prerequisite for this method to work is ensuring that the internal state of the GPIO Filter is completely initialized before clearing the flag, meaning that it has already sent a low-level pulse to the internal GPIO pin, and the flag has been set. The initialization of the GPIO Filter's internal state can be accelerated by providing a higher clock to the GPIO Filter (the IPC Function Clock of the GPIO). After the GPIO Filter is initialized, you can choose the GPIO Filter Clock Source according to your needs.

可以先配置 GPIO 过滤器，再清除标志位，最后配置 GPIO 的中断。这种方法能修复的前提是在清除标志位之前要保证 GPIO 过滤器内部状态初始化完成，已经发送了低电平脉冲给 GPIO 内部引脚，且 flag 已经被置起。可以通过给 GPIO 过滤器较高的 clock(GPIO 的功能时钟) 来加快过滤器内部状态初始化。GPIO 过滤器初始化完成后可以再根据需求选择过滤器的功能时钟源。

GPIO Filter(T_{Filter})can be determined by multiplying the period of Filter's functional clock($T_{FilterClkSrc}$) by the Digital Filter width(N_{DFW}) configured in GPIO_PCR[DFW]. The calculation formula is as follows:

GPIO 过滤器的过滤周期（T_{filter}）可以由过滤器功能时钟源的周期（$T_{FilterClkSrc}$）乘以宽度 GPIO_PCR[DFW]（N_{DFW}）得出，计算公式如下:

$$T_{Filter} = T_{FilterClkSrc} * N_{DFW}$$

Workaround 2 规避方案 2

Disable the GPIO Filter function.

关闭 GPIO Filter 功能。

E300002: [GPIO] Write GPIO registers may clear interrupt flags

Description 描述

When a write operation is performed on a set of GPIO module registers, the write operation also affects the interrupt flag register of the GPIO. This is equivalent to simultaneously performing a write operation on the interrupt flag register of the GPIO.

当对一组 GPIO 模块寄存器进行写操作时，该写操作会同时作用到 GPIO 的中断标志寄存器。行为上相当于同时对 GPIO 中断标志寄存器同时进行了一次写操作。

Reading from the GPIO register has no additional impact.

对于 GPIO 寄存器的读操作并不会有额外的影响。

Example 示例

when GPIOA_PIFR=0x00010001, writing 0x00000001 to GPIOA_PSOR, the PIFR register will become 0x00010000, that is, the lowest bit flag is cleared by mistake, but the 16th bit Flag has no effect because the written data corresponds to the bit 0. Writing to any register in another group, such as GPIOB, will not affect the state of GPIOA.

当 GPIOA_PIFR=0x00010001 时，对 GPIOA_PSOR 写入 0x00000001 时，PIFR 寄存器会变成 0x00010000，也就是最低位的 flag 被错误的清零了，但是第 16 位 Flag 因为写入数据对应比特位 0，则无影响。写入其它组任意寄存器，例如 GPIOB，并不会影响 GPIOA 的状态。

Workaround 规避方案

Before writing to the GPIO register, read the interrupt register status. For GPIO output operations, use the PSOR and PCOR registers for bitwise operations. When operating the PDOR, ensure that the corresponding bit of the GPIO input status pin is written to 0.

写入 GPIO 寄存器前先读取中断寄存器状态，对于 GPIO 输出操作采用 PSOR 和 PCOR 寄存器按位操作，操作 PDOR 时确保 GPIO 输入状态引脚对应比特写 0。

E300003: [GPIO] When SXOSC is selected as GPIO filter clock, there may be an unexpected interrupt after GPIO falling edge wake-up

Description 描述

When using GPIO to wake up LOWPOWER, if the GPIO is configured for falling edge wake-up and the clock of the Filter is selected as SXOSC. So after GPIO wakes up LOWPOWER, GPIO may also generate an unexpected interrupt.

当使用 GPIO 的下降沿来唤醒处于低功耗模式下的 MCU 时，且过滤器的时钟选择为 SXOSC，那么在唤醒后，MCU 可能还会进一次意外的中断。

Workaround 规避方案

When using GPIO to wake up LOWPOWER with a falling edge, avoid using SXOSC as the Filter clock.

在使用 GPIO 的下降沿唤醒 MCU 时，避免使用 SXOSC 作为过滤器的时钟源。

E300004: [GPIO] Slow transition edges (both rising/falling) on GPIO inputs can induce spurious interrupts

Description 描述

Slow transition edges (both rising/falling) on GPIO inputs can induce spurious interrupts.

当 GPIO 输入端的上升沿和下降沿过渡速度过缓时，可能引发伪中断。

Workaround 1 规避方案 1

Enable PCTRL digital Filter.

打开引脚数字滤波器功能。

Workaround 2 规避方案 2

The rise/fall input transition time of GPIO must be ensured to be less than 5μs.

GPIO 的上升/下降输入过渡时间必须保证小于 5 微秒。

E403001: [SPI] RXFIFO overflow flag logic error

Description 描述

When the FIFO depth is N, SPI will only set the overflow flag of the RXFIFO after receiving N+2 data.

当 FIFO 深度为 N 时，SPI 在接收 N+2 个数据之后接收 FIFO 的溢出标志才会置起。

Workaround 1 规避方案 1

Don’t use receive FIFO overflow flag and its interrupt.

不要使用接收 FIFO 溢出标志及其中断。

Workaround 2 规避方案 2

Users should follow this rule when using receive FIFO overflow flag and its interrupt.

用户按照这一规则去使用接收 FIFO 溢出标志及其中断。

E403002: [SPI] TXCFG register read value keep old after writing

Description 描述

When changing the TXCFG configuration, immediately reading back will return the old value and it won't be updated even if read continuously for a long time.

当改变 TXCFG 配置后，立即回读会发现读到的还是旧值，一直读也不会更新。

Workaround 规避方案

After writing the TXCFG register, wait for data synchronization(around 3 functional clock cycles), and then read any other register once before reading back the TXCFG register.

写完 TXCFG 寄存器之后，延时等待数据同步（约 3 个功能时钟周期）, 然后在回读 TXCFG 寄存器之前，先读一次其它任意寄存器。

E403003: [SPI] In SPI master mode, enabling both PCS continuous mode and TX mask simultaneously will result in continuous clock output

Description 描述

When the SPI module operates as master with both PCS continuous mode and TX Mask enabled, the master will continuously output clock until either PCS continuous mode or TX Mask (or both) is disabled, or until the RxFIFO is filled with data.

当 SPI 模块作为主机且同时使用连续模式和 Tx Mask 功能时，主机将一直输出 clock，直到关闭连续模式和 Tx Mask 功能中的一个或全部，或者 RxFIFO 被填满数据。

Workaround 1 规避方案 1

In SPI multi-line master mode, writing 0xFFFFFFFF to the DATA register can be used as an alternative to the TX Mask function.

SPI 主机在多线模式下，往 DATA 寄存器写入 0xFFFFFFFF 方式替代 Tx Mask 功能。

Workaround 2 规避方案 2

In SPI single-line or multi-line master mode, GPIO can be used as an alternative to the PCS continuous function.

SPI 主机在多线或者单线模式下，使用 GPIO 控制 PCS 来替代连续模式。

E405001: [UART] Clear match flag bit mismatch

Description 描述

Uart module INTF[MATIF] clear logic error, normal use of write 1 clear 0 can not clear this flag bit.

Uart 模块中 INTF[MATIF] 清除逻辑错误，正常使用写 1 清 0 无法清除此标志位。

Workaround 规避方案

Since INTF[MATIF] and INTF[RXEDGEIF] are both cleared by writing bit 10, the user should pay attention to whether both bits are valid at the same time when checking the flag bits, if not valid at the same time, then write bit 10 is used to clear one of the two bits; if pulled high at the same time, then it is necessary to balance which one is more critical; if interrupts are turned on, then it is necessary to determine in the corresponding interrupts If an interrupt is enabled, it is necessary to determine in the corresponding interrupt whether the other bit is also high.

由于 INTF[MATIF] 及 INTF[RXEDGEIF] 均由写 bit10 来清除，所以用户在检查标志位时应同时注意这两位是否均有效，若不同时有效则使用写 bit 10 来清除两个 bit 位中的一个；若同时拉高则需要平衡哪个更为关键；如果开启了中断，则要在相应的中断中判断另外一位是否也为高。

E407001: [I2C] In I2C slave mode, turning on tx stall may cause I2C master arbitration to fail

Description 描述

When an I2C module operates as a slave and the TX stall function is enabled, if the master sends a read command and the slave hasn't had time to write data to the TX FIFO, the slave will hold both the SCL and SDA lines low. This state is maintained until the TX FIFO is populated with data. However, if the most significant bit of the data written to the TX FIFO is 1, SDA line will be pulled up, and SCL line will be released after one cycle of I2C peripheral clock, at this time SCL line also will be pulled up. If the rising edge of SDA line occurs during SCL line's high level, it will be considered as a stop signal, which will cause the arbitration failure.

当 I2C 模块作为从机且打开 Tx Stall 功能的时候，主机发送读的命令，从机未来得及往 Tx FIFO 里填写数据，此时从机会将 SCL 和 SDA 线拉低，一直到 Tx FIFO 中被填写数据；若填写的数据最高位为 1，则会将 SDA 线拉高，然后延迟一个 I2C 外设时钟释放 SCL 线，此时 SCL 线会被拉高，如果 SDA 线拉高时的上升沿出现在 SCL 线高电平的时候，那么硬件认为是终止信号，导致仲裁失败，如图所示。

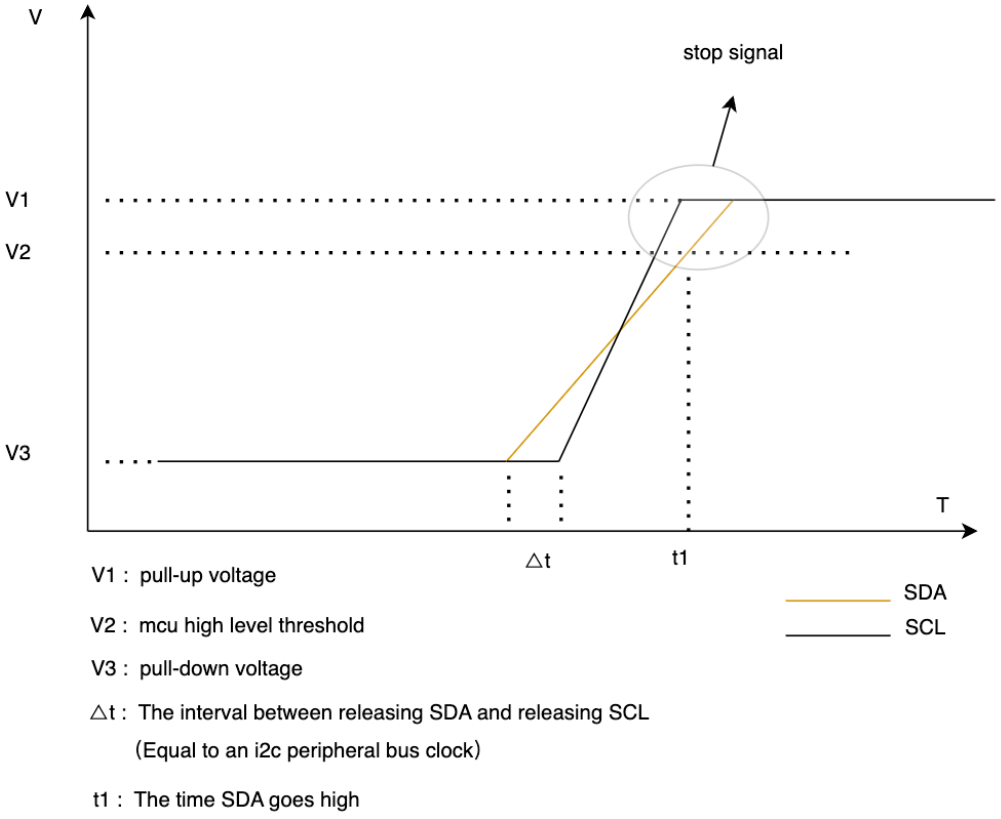


Figure 2: SDA SCL 时序说明

Workaround 1 规避方案 1

As an I2C slave, the module preloads data into the Tx Buffer before the master's read operation, thus preventing the Tx Stall feature from engaging and avoiding simultaneous

release of SCL and SDA from low states.

I2C 模块作为从机，在 I2C 主机进行读的操作的时候，从机提前将数据写入 Tx Buff，这样 Tx Stall 功能就不会生效，避免了 SCL 和 SDA 同时从低电平被释放。

Using this method requires the I2C to write to the Tx FIFO promptly, necessitating a higher priority for the I2C and ensuring it is not interrupted for extended periods.

用上面的方法可能需要 I2C 及时往 Tx FIFO 里写，这样就需要 I2C 有较高的优先级，且不能长时间被打断。

Workaround 2 规避方案 2

If the user still uses the Tx stall function, the highest bit of data sent is still 1, then the external circuit is required to satisfy the requirement that in standard mode (by adjusting the pull-up resistor R_p or the bus capacitor C_b) the SDA should be pulled high at least 250ns before SCL goes high, in fast mode the SDA should be pulled high at least 100ns before SCL goes high, and in upgraded fast mode the SDA should be pulled high at least 50ns before SCL goes high. SDA should be pulled high at least 50ns before SCL is high in fast-mode, and at least 50ns before SCL is high in fast-mode pulse.

若用户仍然使用 Tx stall 功能，此时发送数据的最高位仍然为 1，则需要外部电路满足在标准模式下（通过调整上拉电阻 Rp 或者总线电容 Cb）SDA 要在 SCL 为高前至少 250ns 拉高，在快速模式下 SDA 要在 SCL 为高前至少 100ns 拉高，在升级快速模式下 SDA 要在 SCL 为高前至少 50ns 拉高。

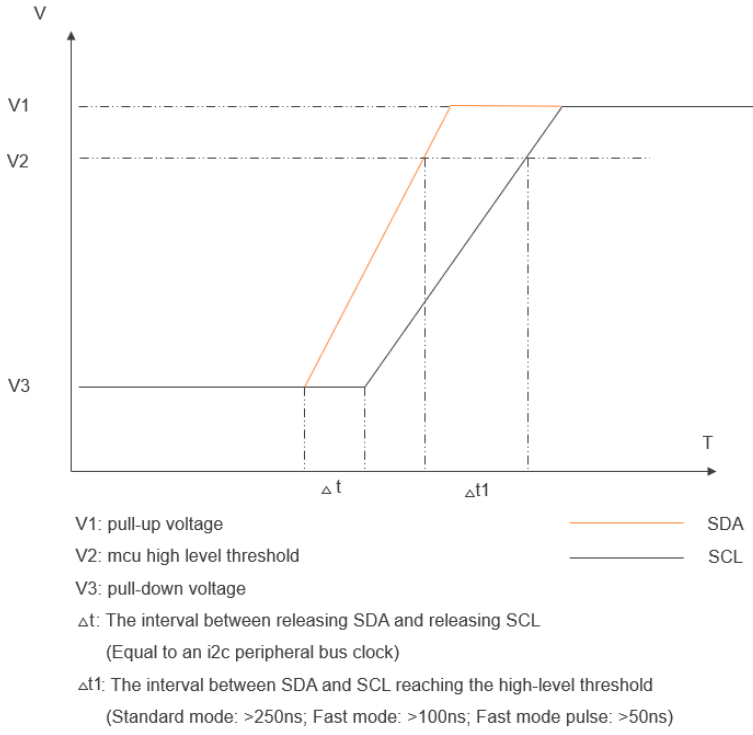


Figure 3: workaround 2

E502001: [LPTMR] When polling to read CCF, there is a small probability of reading incorrect flag information

Description 描述

When polling to read the CCF of LPTMR, there is a small probability of reading the wrong CCF. This situation occurs when the CCF is pulled up and the CCF is read exactly, and its probability of occurrence increases with the increase of the bus clock frequency/function clock frequency of LPTMR.

在轮询读取 LPTMR 的 CCF 时，有较小的概率会读到错误的 CCF，这种情况出现在 CCF 拉起时正好读 CCF，且它的发生概率随着 LPTMR 的总线时钟频率/功能时钟频率提高而提高。

Workaround 1 规避方案 1

After the interrupt is raised, reading the CCF again will not read the wrong CCF.

中断升起后再读 CCF 就不会读到错误的 CCF。

Workaround 2 规避方案 2

During polling, CCF can be read twice (to avoid reading metastable states). When the values of CCF read twice meet expectations, it is determined that CCF has risen.

在轮询时，可以读两次 CCF（避免读到亚稳态），当两次读的 CCF 的值都符合预期时，判定为 CCF 升起。

E503001: [eTMR] 100% duty cycle can not be generated through configuring VAL0 and VAL1 register

Description 描述

100% duty cycle can not be generated through configuring VAL0 as initial value and VAL1 as MOD value when to output PWM.

当输出 PWM 时，100% 占空比无法通过配置 VAL0 为初始值和 VAL1 为 MOD 得到。

Workaround 规避方案

Achieve 100% duty cycle through configuring CHMASK register. The way is to configure channel mask enable(CHMASK[CHnM]) and mask value(CHMASK[CHnMV]).

通过配置 CHMASK 寄存器来实现 100% 占空比。配置方式为配置某一通道的使能 (CHMASK[CHnM]) 和该通道的 MASK 值 (CHMASK[CHnMV])。

E503003: [eTMR] The channel 2-7 DMA requests of eTMR1 and eTMR2 will not be cleared by DMA done

Description 描述

Channel 2-7 of eTMR1 and eTMR2 will trigger DMA requests continuously since the DMA requests can not be cleared by DMA done. While all of channels of other eTMRs, channel 0-1 of eTMR1 and eTMR2 are normal.

eTMR1 和 eTMR2 的通道 2 到 7 会一直触发 DMA 请求，因为 DMA 传输完成后不会把 DMA 请求清掉。而其他 eTMR 的所有通道以及 eTMR1 和 eTMR2 的通道 0 和 1 都正常。

Workaround 规避方案

For problematic channels, user can use interrupt handler instead of DMA transfer.

对于有问题的通道，用户可以使用中断处理代替 DMA 传输。

E503005: [eTMR] The channel flag will be set if channel capture event occurs before counter enable

Description 描述

The channel flag will be set if channel capture event occurs before counter starts.

如果在计数器开启之前通道捕获事件发生，那么通道标志位会被置起。

So if interrupt or DMA enables before eTMR enables, it will cause the interrupt service routine or DMA request to respond immediately once the counter starts, and the first capture value is always 0.

所以如果中断或者 DMA 在 eTMR 使能之前使能了，这将导致一旦计数器开启中断处理或者 DMA 请求会立即响应，第一次的捕获值总是为 0.

Workaround 1 规避方案 1

Clear the channel flag before enabling the counter.

在开启计数器之前清掉通道事件的标志位。

Workaround 2 规避方案 2

Enable counter before enabling channel interrupt.

先使能 eTMR，打开计数器，再打开通道中断使能和中断服务。

E503009: [eTMR] Write 0 to LDOK bit will clear this bit

Description 描述

Setting LDOK bit is generally used to reload the value of the shadow registers, and normally it is automatically cleared by the hardware after loading is complete, so this bit also can be used to determine whether the loading is complete.

置位 LDOK 一般用于更新影子寄存器的值，正常情况下该位在加载完成之后会硬件自动清零，因此可以通过此位来判断加载是否完成。

However, actually it will be cleared if writes 0 to this bit after the bit is set.

然而实际情况是该位在置起后，如果软件写 0 则会将其清零。

Workaround 规避方案

Software should not write 0 to this bit at any time. SYNC[CLDOK] bit field is used to clear LDOK bit in normal.

在任何时候不应该对该位写 0。正常情况下 SYNC[CLDOK] 位是用来清 LDOK 位的。

E509001: [RTC] Alarm/Seconds/Overflow flag will not be set again after write 1 clear

Description 描述

After writing 1 to clear the alarm/seconds/overflow flag, the alarm/seconds/overflow flag will remain clear and will not be set again.

对 RTC 的 alarm/seconds/overflow 标志位进行写 1 清零后，RTC 的 alarm/seconds/overflow 标志位将会保持清除状态，且不会再次置起。

Workaround 规避方案

After clearing the alarm/seconds/overflow flag, execute a register access (either read or write). For example, change the operation of clearing the flag to: write 1 first and then write 0, or write 1 first and then read back.

在清除完 alarm/seconds/overflow 标志位后进行一次任意的寄存器访问（读或者写都可以）。例如，可以将清除标志位的操作改为：对标志位先写 1 再写 0 或者对标志位先写 1 再读一次。

E600004: [ADC] A reduction in VDD voltage to 2.7V may lead to a performance degradation in ADC

Description 描述

When the VDD voltage drops to 2.7V, the Effective Number of Bits (ENOB) of the ADC will decrease by 1 bit.

当 VDD 电压下降到 2.7V 时，ADC 的有效位数 (ENOB) 将下降 1bit。

Workaround 规避方案

To ensure optimal ADC performance, it is recommended that customers kepp the VDD voltage above 2.97V.

为保证 ADC 性能，建议客户确保 VDD 电压在 2.97V 以上。

E600005: [ADC] When the ADC bus clock frequency differs greatly from the function clock frequency, the problem of multiple interrupts may occur

Description 描述

When the ADC function clock and bus clock frequency gap is large (depending on the interrupt and handle the interrupt exit time is less than the bus clock and function clock multiples), if you open the corresponding interrupt, this time the interrupt flag bit is pulled high, and then enter the corresponding interrupt, the user in the exit of the interrupt will generally write 1 to clear the corresponding flag bit, and then at this time due to the difference between the frequency of the bus and the function clock frequency Then, due to the large difference between the bus frequency and the function clock frequency, it is not possible to synchronize the clearing to the function clock domain in time, so the flag bit is not effectively cleared, which leads to repeatedly entering the same interrupt after exiting the interrupt.

当 ADC 功能时钟与总线时钟频率差距较大时 (具体取决于进入中断且处理完中断退出时的时间是否小于总线时钟与功能时钟的倍数)，若开启相应中断，此时中断标志位拉高，然后进入相应中断，用户在退出中断时一般会写 1 清零来清除相应标志位，然后此时由于总线频率与功能时钟频率相差较大，未能及时同步清除到功能时钟域，所以标志位并未有效清除，从而导致在退出中断之后反复进入同一个中断。

Workaround 规避方案

If the user is not sure whether the processing time of each interrupt is less than the relationship between the bus clock and the function clock multiplier, it is recommended that the user check whether the corresponding flag bit is actually cleared when the interrupt service program exits, to prevent the same interrupt from repeatedly entering the problem.

若用户无法确定每次进中断处理的时间是否小于总线时钟与功能时钟倍数的关系，此时建议用户在中断服务程序退出时检查相应标志位是否确实被清除，防止同一中断反复进入的问题。

E600007: [ADC] TMU Trigger Source ADC0_COCO for Monitoring ADC Conversion Status

Description 描述

Upon completion of a channel conversion, the status flag STS[EOC] is set and can be cleared either by a write-1-to-clear (W1C) operation or by reading the conversion result register. The TMU trigger source ADC0_COCO is derived directly from the STS[EOC] status bit. When this trigger signal is output to a pad, it remains asserted at logic level 1 if no read operation or explicit W1C action is performed to clear the EOC status. This behavior prevents the trigger signal from being pulsed for each conversion completion, thereby hindering real-time monitoring of the ADC conversion process.

当通道转换完成后，状态标志位 STS[EOC] 会被置位，该标志可通过写 1 清除（W1C）操作或读取转换结果寄存器来清零。TMU 触发源 ADC0_COCO 直接源自 STS[EOC] 状态位。当该触发信号被输出到引脚时，如果未执行读取操作或显式的 W1C 操作来清除 EOC 状态，该信号将保持为逻辑电平 1。此行为导致触发信号无法在每次转换完成时产生脉冲，从而影响对 ADC 转换过程的实时监测。

Workaround 规避方案

To ensure the trigger signal behaves as a pulse for each conversion event, the STS[EOC] status bit must be cleared in a timely manner. This can be achieved by one of the following methods:

Performing a software write-1-to-clear (W1C) operation on the STS[EOC] bit, preferably within the ADC interrupt service routine (ISR) if interrupts are used. Initiating a DMA read operation to the conversion result register, which automatically clears the EOC status.

为确保触发信号在每次转换事件时表现为脉冲，必须及时清除 STS[EOC] 状态位。可采用以下方法之一：

在软件中执行写 1 清除（W1C）操作清除 STS[EOC] 位（若使用中断，建议在 ADC 中断服务例程中完成）；通过 DMA 对转换结果寄存器的读取操作自动清除 EOC 状态；

E706001: [CRC] Writing high 16 bits data to DATA register is invalid

Description 描述

When using CRC to calculate the checksum, using 16-bit access way to write data to high 16 bits of DATA register is invalid, and the CRC will not receive this data. (32-bit access/low 16-bit access and any 8-bit access are valid)

使用 CRC 计算校验码时，使用 16 位访问方式写数据到 DATA 寄存器的高 16 位是无效的，CRC 将不会收到该数据。（32 位访问/低 16 位写以及任意 8 位访问都是有效的）

Workaround 规避方案

Avoid writing high 16 bits data during calculation and only use other valid access way.

计算时避免高 16 位的写入，而使用其他有效的访问方式。

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