Standardized Information for Process/Product Change Notification (PCN)

Form provided by ZVEI - Revision 5.0

1. PCN basic data			
1.1 Company	云途 YUNTU	Jiangsu Yuntu Microelectronics Co., Ltd.,	
1.2 PCN No.		YT-PCN-2511B	
1.3 Title of PCN		MCU Errata Correction and Test Flow Upgrade Notification	
1.4 Product Category		Active Components - Integrated Circuits	
1.5 Issue date		2026/01/12	
1.6 PCN revision history (optional)		1.7 Issue date of previous revision (optional)	1.8 Delta to previous revision (optional)

2. PCN Team		
2.1 Contact supplier		
2.1.1 Name	Guangyue Gu	
2.1.2 Phone	18616949588	
2.1.3 Email	pcn@ytmicro.com	
2.2 Team supplier (optional)		
2.2.1 Name (optional)	2.2.2 Phone (optional)	2.2.3 Email (optional)

3. Changes			
No.	3.0 Ident	3.1 Category	3.2 Type of change
#1	SEM-DS-01	DATA SHEET	Change of datasheet parameters/electrical specification (min./max./typ. values) and/or AC/DC specification
#2	SEM-DS-03	DATA SHEET	Specification of additional parameters
#3	SEM-DE-02	DESIGN	Design changes in routing .
#4	SEM-TF-01	TEST FLOW	Move of all or part of electrical wafer test and/or final test to a different test site.

4. Description of change		
	Old	New
Change #1	POR (Power-On Reset) Circuit Configuration: Typical POR threshold voltage is 0.7V. The user has the capability to disable the BOR (Brown-Out Reset) circuit.	POR/BOR Circuit Parameter and Configuration Update: New typical POR threshold voltage is adjusted to 1.8V. The BOR circuit is now permanently enabled, and user applications cannot disable it.
Change #2	Flash Control Register Bit Definition: The Flash Readonly bit (EFM->CTRL[READONLY]) is currently reserved for internal use.	Flash Control Register Bit Definition: The Flash Readonly bit (EFM->CTRL[READONLY]) is now released and open for user configuration/usage. Note: this bit always returns 0 when read.
Change #3	General Purpose Input/Output (GPIO) Specification Enhancement: GPIO voltage hysteresis noise immunity voltage is about 50mV.	General Purpose Input/Output (GPIO) Specification Enhancement: New GPIO voltage hysteresis noise immunity voltage is increased to 500mV.
Change #4	Product Test Flow Optimization: High/Low temperature testing is performed under the Final Test (FT) flow.	Product Test Flow Optimization: High/Low temperature testing is shifted and performed under the Chip Probe Test (CP) flow.
4.1 Anticipated impact on form, fit, function, reliability or processability?	**1. POR/BOR Circuit Change** **Impact on Function**: The change in the POR threshold voltage (from 0.7V to 1.8V) may affect the MCU's power-up and power-down sequence in the user application. The permanently enabled BOR enhances system robustness against power glitches, but removes user control over this feature. **Action Required**: Customer must evaluate the new POR threshold against their power supply management requirements. **2. Flash Readonly Bit Release** **Impact on Function**: The release of the EFM->CTRL[READONLY] bit provides additional functionality for user-configurable Flash erase and write protection. No negative impact is anticipated. **3. GPIO voltage hysteresis noise immunity** **Impact on Function**: The increase in GPIO input hysteresis (from 50mV to 500mV) significantly improves the noise immunity of the digital inputs. No negative impact is anticipated. **4. High/Low Temperature Test Flow Adjustment** **Impact on Reliability/Quality**: The change in test location from Final Test to Chip Probe Test is an internal process optimization and does not affect the product's electrical specifications or final quality standards.	
4.2 Reference parts with customer number (optional)		

5. Reason / motivation for change	
5.1 Motivation	**1. Enhance Product Reliability and Stability**: a. Hardware Design Optimization (Change #1 & #3): Corrects two known design errata (E110001 and E300004). By adjusting POR/BOR parameters and increasing GPIO hysteresis, the MCU's startup robustness and signal noise immunity are significantly improved in challenging operating environments. **2. Enable New User Functionality** (Change #2): Enables the Flash Readonly protection bit in the EFM control register to provide customers with an additional layer of hardware-based application code and data protection. **3. Optimize Manufacturing Test Flow** (Change #4): Relocates the High/Low temperature test to Chip Probe Test (CP). This leverages a more controlled thermal environment for earlier and more reliable testing of the bare die, thereby enhancing the overall quality assurance of the final product.
5.2 Additional explanation (optional)	

6. Marking of parts / traceability of change	
6.1 Description	The batch NO. marking ends with the number "2" and DC>=2529 

7. Timing / schedule		
7.1 Date of qualification results	**2025/10/25**	
7.2 Last order date (optional)		
7.3 Last delivery date (optional)		
7.4 Intended start of delivery	**2026/04/09**	Quantity <10K (LE05 48&64PIN) can be expected from the end of January, and mass production for all types can be expected by the end of March.
7.5 Qualification samples available?	Available after 2025/10/31	
7.6 Customer feedback required until	**2026/04/09**	

8. Qualification / validation				
8.1 Description (e.g. qual. plan/report, AEC-Q...)	According to ZVEI and AEC-Q100 requirement， test item are A4/E2/E3/E4/E5/E7, the result is pass，reports can refer to attachment			
8.2 Qualification report and qualification results	available (see attachement)	**issue date**	**2025/10/31**	

9. Input to customer for risk assessment process

10. Attachments (e.g. new datasheet, additional documentation, pictures, process flow, sample plan, ...)
Relative qualification reports please refer to attachemnts: Additional documentations please refer to the link below: https://doc.ytmicro.com/pcn/yt_pcn_2511b/

11. Affected parts									
11.1 Current						11.2 New (if applicable)			
11.1.1 Customer Part No.	11.1.2 Supplier Part Name	11.1.3 Supplier Part No. (optional)	11.1.4 Package Name	11.1.5 Part Description (optional)	11.1.6 Additional Part Information (optional)	11.2.2 Supplier Part Name	11.2.3 Supplier Part No. (optional)	11.2.4 Package Name	11.2.6 Additional Part Information (optional)
	YTM32B1LE05H0MLHT		LQFP64			YTM32B1LE05H0MLHT		LQFP64	
	YTM32B1LE05H0MLFT		LQFP48			YTM32B1LE05H0MLFT		LQFP48	
	YTM32B1LE05H0MLET		LQFP32			YTM32B1LE05H0MLET		LQFP32	
	YTM32B1LE05H0MFMR		QFN32			YTM32B1LE05H0MFMR		QFN32	
	YTM32B1LE04H0MLFT		LQFP48			YTM32B1LE04H0MLFT		LQFP48	
	YTM32B1LE04H0MLET		LQFP32			YTM32B1LE04H0MLET		LQFP32	
	YTM32B1LE04H0MFMR		QFN32			YTM32B1LE04H0MFMR		QFN32	
	YTM32B1LE05H0MLHR		LQFP64			YTM32B1LE05H0MLHR		LQFP64	
	YTM32B1LE05H0MLER		LQFP32			YTM32B1LE05H0MLER		LQFP32	
	YTM32B1LE05H0MFMIR		QFN32			YTM32B1LE05H0MFMIR		QFN32	

过程/产品变更通知（PCN）的标准化信息

1. PCN基础信息		
1.1公司名	云途 YUNTU	江苏云途半导体有限公司
1.2 PCN No.		YT-PCN-2511B
1.3 PCN 标题		MCU 勘误修正与测试流程升级通知
1.4 产品种类		有源器件-集成电路
1.5 发布时间		2026/1/12

1.6 PCN版本历史（选填）	1.7 历史版本的发布时间（选填）	1.8 历史版本详述（选填）

2. PCN 团队	
2.1 供应商联络窗口	
2.1.1 姓名	顾光跃
2.1.2 电话	18616949588
2.1.3 邮箱	pcn@ytmicro.com

2.2 供应商团队（选填）

2.2.1 姓名（选填）	2.2.2 电话（选填）	2.2.3 邮箱（选填）

3. 变更			
No.	3.0 识别号	3.1 种类	3.2 变更类型
#1	SEM-DS-01	DATA SHEET	数据手册参数/电气规范变更（最小/最大/典型值），
#2	SEM-DS=03	DATA SHEET	增加额外参数
#3	SEM-DE-02	DESIGN	设计走线改动
#4	SEM-TF-01	TEST FLOW	将全部或部分晶圆电性测试和/或成品最终测试转移至其他

4.变更描述		
	旧	新
Change #1	POR（上电复位）电路配置: 典型的 POR 门限电压为 0.7 V。用户可根据需要关闭 BOR（掉电/欠压复位）电路。	POR/BOR 电路参数及配置更新: 新的典型 POR 门限电压已调整为 1.8 V。BOR 电路将被永久使能，用户应用程序无法再将其关闭。
Change #2	Flash 控制寄存器位定义: Flash 只读位（EFM->CTRL[READONLY]）目前保留供内部使用。	Flash 控制寄存器位定义: Flash 只读位（EFM->CTRL[READONLY]）现已开放给用户进行配置和使用。 注意： 该位在读取时始终返回 0。
Change #3	通用输入/输出（GPIO）规格增强: GPIO 的电压迟滞噪声抑制电压约为 50 mV。	通用输入/输出（GPIO）规格增强: 新的 GPIO 电压迟滞噪声抑制电压已提升至 500 mV。
Change #4	产品测试流程优化: 高/低温测试在最终测试（FT）流程下进行。	产品测试流程优化: 高/低温测试已调整至芯片探针测试（CP）流程下进行。
4.1 对表单、贴合度、功能、可靠性或可加工性预计会产生何种影响?	1. POR/BOR 电路变更 • 功能影响： POR 门限电压从 0.7 V 调整为 1.8 V，可能会影响用户应用中 MCU 的上电和断电顺序。BOR 电路永久使能可增强系统对电源扰动的鲁棒性，但用户将无法再控制该功能。 • 所需操作： 客户需评估新的 POR 门限是否符合其电源管理要求。 2. Flash 只读位开放 • 功能影响： EFM->CTRL[READONLY] 位的开放，为用户提供了可配置 Flash 擦写保护的新功能。不会产生负面影响。 3. GPIO 电压迟滞噪声抑制增强 • 功能影响： GPIO 输入迟滞由 50 mV 提升至 500 mV，显著提高了数字输入的抗噪声能力。不会产生负面影响。 4. 高/低温测试流程调整 • 可靠性/质量影响： 测试环节从最终测试（FT）调整至芯片探针测试（CP）属于内部流程优化，不影响产品电气规格及最终质量标准。	
4.2 标注客户编号的参考件（选填）		

5.变更的理由/动机	
5.1 动机	1. 提升产品可靠性与稳定性: • 硬件设计优化（变更 #1 & #3）： 修正了两个已知设计勘误（E110001 和 E300004）。通过调整 POR/BOR 参数及增加 GPIO 迟滞，显著提升了 MCU 在苛刻工作环境下的上电启动稳健性和信号抗噪能力。 2. 启用新用户功能（变更 #2）： • 开放 EFM 控制寄存器中的 Flash 只读保护位，为客户提供额外的硬件级应用程序代码和数据保护功能。 3. 优化制造测试流程（变更 #4）： • 将高/低温测试调整至芯片探针测试（CP），利用更可控的热环境对裸芯片进行早期和更可靠的测试，从而提升最终产品整体质量保证水平。
5.2 补充说明（选填）	

6. 变更的零件标识/可追溯性		
6.1 描述	批号以 数字 “2” 结尾 且 DC ≥ 2529。	

7. 时效/时间表		
7.1 获得产品合规性结果的时间	**2025/10/25**	
7.2 最后下单的时间（选填）		
7.3 最后交货的时间（选填）		
7.4 预计交付时间	**2026/04/09**	1 月底可供应少于1万片(LE05 48＆64PIN)，3 月底可实现全型号量产。
7.5 是否能提供合规的样品?	2025/10/31之后	
7.6 需求客户反馈的截止时间	**2026/04/09**	

8. 资格认证/验证				
8.1 描述 （例如：认证计划/报告，AEC-Q）	根据 ZVEI 和 AEC-Q100 要求，测试项目包括 A4 / E2 / E3 / E4 / E5 / E7，测试结果均通过，相关报告请参见附件			
8.2 资格审查报告及审查结果	已完成	发行时间	2025/10/31	

9. 客户风险评估流程的输入信息

10. 附件 （例如：新的规格书，补充文档，图片，工艺流程图，样品计划，.....）
相关认证报告请参考附件： 其他文档请点击下方链接获取： https://doc.ytmicro.com/pcn/yt_pcn_2511b/

11. 受影响的零件									
11.1 现况						11.2 新增内容（如适用）			
11.1.1 客户零件号	11.1.2 供应商零件名称	11.1.3 供应商料号（选填）	11.1.4 封装名	11.1.5 零件描述（选填）	11.1.6 额外的零件信息（选填）	11.2.2 供应商零件名	11.2.3 供应商零件号（选填）	11.2.4 封装名	11.2.6 额外的零件信息（选填）
	YTM32B1LE05H0MLHT		LQFP64			YTM32B1LE05H0MLHT		LQFP64	
	YTM32B1LE05H0MLFT		LQFP48			YTM32B1LE05H0MLFT		LQFP48	
	YTM32B1LE05H0MLET		LQFP32			YTM32B1LE05H0MLET		LQFP32	
	YTM32B1LE05H0MFMR		QFN32			YTM32B1LE05H0MFMR		QFN32	
	YTM32B1LE04H0MLFT		LQFP48			YTM32B1LE04H0MLFT		LQFP48	
	YTM32B1LE04H0MLET		LQFP32			YTM32B1LE04H0MLET		LQFP32	
	YTM32B1LE04H0MFMR		QFN32			YTM32B1LE04H0MFMR		QFN32	
	YTM32B1LE05H0MLHR		LQFP64			YTM32B1LE05H0MLHR		LQFP64	
	YTM32B1LE05H0MLER		LQFP32			YTM32B1LE05H0MLER		LQFP32	
	YTM32B1LE05H0MFMIR		QFN32			YTM32B1LE05H0MFMIR		QFN32	